arasan
Total IP Solutions

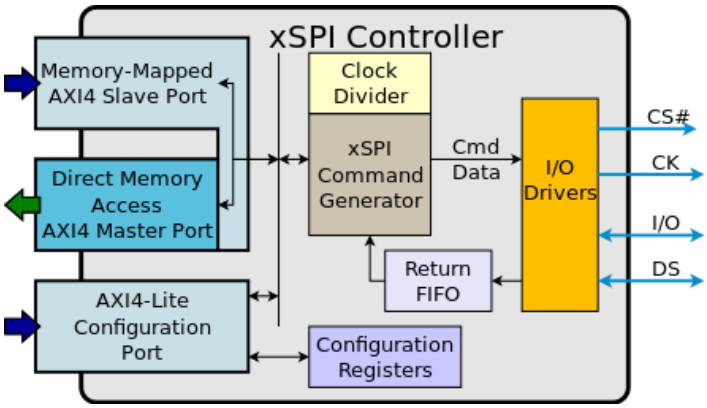
PRODUCT OVERVIEW

SUREBOOT™ XSPI MASTER IP

OVERVIEW

Arasan Chip Systems, the leading provider of IP for Mobile Storage Standards, presents its latest xSPI Master IP for access to NOR Flash Devices. This Universal NOR Flash IP supports a variety of NOR Devices and multiple Protocols, combines ease of use with high reliability, low power and speed under all conditions, including automotive applications.

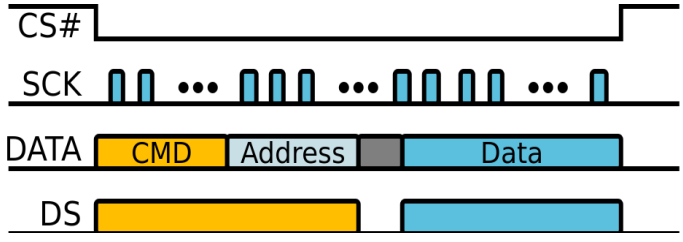
The xSPI master IP supports the xSPI JESD251 standard from a standard AXI4 slave interface, and also features backwards compatibility support for Octal SPI, QSPI, DSPI, and SPI interfaces. The xSPI Master IP also supports JEDEC SFDP Standard. It is designed so that a user design may immediately access memory from the xSPI device in SPI mode, or alternatively issue a command to switch to any other mode. Additionally, a DMA command may be issued to copy memory from the xSPI device to anywhere else on the bus.



PRODUCT DETAILS

SPI PROTOCOLS

The xSPI Master Core is built around the xSPI protocol, capable of transferring 16-bits on every 200MHz clock. It remains backwards compatible with the prior Octal SPI, QSPI, Dual SPI and SPI standards.



KEY BENEFITS

Arasan xSPI Controller IP is an universal controller supporting all NOR Flash Devices.

Total xSPI IP Solution includes xSPI Device, HDK & SW

Low Gate Count & Low Power

KEY FEATURES

- JESD 251 compliant
  - Protocols 1 & 2
- JEDEC SFDP Compliant
- 8b and 4b xSPI
  - -- Octal SPI, QSPI, DSPI
  - -- Resets into SPI mode
  - -- 24 or 32b addressing
  - -- User selectable cmds
  - -- XIP high speed support
- AXI4 Execute in Place
  - -- Parameterized width
  - -- Full & Narrow burst
  - -- Max Bus Throughput
- AXI4 DMA Master
  - -- High speed bulk operations
  - -- Parameterized width
  - -- Full & Narrow burst
  - -- Max bus throughput
  - -- Read Straight to RAM
- AXI4-Lite Configuration Port
  - -- Low level command access
- JESD SFDP support
- High level software library

AXI4 SLAVE

The primary interface to this xSPI master IP is a memory mapped AXI4 slave port. Reads from this port will automatically read from the attached xSPI memory. Further, the xSPI master IP is optimized for reading, and therefore capable of maintaining high read speeds that are not limited by crossing AXI burst read boundaries.

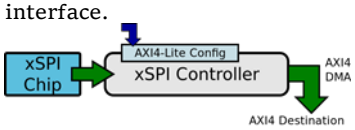
AXI4-LITE SLAVE

Moving from one mode or clock configuration to another requires interacting with a set of control registers. These control registers allow the xSPI IP to be reconfigured from one mode and clock rate to another. It also allows adjusting any clock-rate dependent parameters of the underlying device interface--required by many QSPI flash devices.

The AXI4-Lite slave port also offers access to a raw, low-level device command control port. This provides user code with access to arbitrary xSPI commands which may be device specific. To maintain xSPI device abstraction, a software library is provided together with the xSPI IP to both demonstrate how to use this low-level library as well as to document and support user access to these functions.

AXI4 DMA MASTER

Finally, this xSPI IP comes with an internal Direct Memory Access controller with an AXI4 master interface.



This DMA controller makes it possible to copy data from the xSPI interface in an unattended fashion. Using this interface, data may be read from the xSPI master interface and written to any other memory addressable by the DMA core.

XSPI IP DELIVERABLES

- Verilog RTL Code
- Homogenous Verilog Test Environment
- Optional UVM Test Environment
- Synthesys Scripts
- xSPI Emulator suitable for integration testing
- Software Configuration Library
- User Guide
- Software configuration library

arasan
Total IP Solutions

ADDRESS 2150 N. First St. Ste #240 San Jose CA 95131
PHONE 408 – 282 – 1600 EMAIL: sales@arasan.com
PLEASE VISIT WWW.ARASAN.COM FOR A DIRECTORY OF ALL OUR IP