# All about MIPI C-PHY℠ and MIPI D-PHY℠

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# MIPI PHY LAYERS

The MIPI physical layers are primarily developed to support the interconnections within the mobile devices, focus being on camera and display. The MIPI PHY layer was introduced by the MIPI Alliance that was established to provide a core collection of standard approaches that would enable mobile device manufacturers to procure components from various suppliers, better optimize the performance of their designs, and accelerate the distribution of their products to end users.

The MIPI PHY layer is one of the six fundamental application areas MIPI Alliance specifications serve. The specifications are available as individual interfaces, enabling companies to adopt those that meet their needs. Under the MIPI Alliance, available PHY layers are MIPI A-PHY℠, MIPI C-PHY℠, MIPI D-PHY℠ and MIPI M-PHY℠.

The MIPI C-PHY℠ and MIPI D-PHY℠ is mainly used for the camera and display interfaces in the mobile devices and It has since been the industry's main high-speed PHY solution for these mobile applications. It is often used in combination with the MIPI Camera Serial Interface-2 (CSI-2®) and MIPI Display Serial Interface (DSI®) protocol specifications. MIPI D-PHY℠ satisfies the stringent specifications of cell phone architecture, including low power, low noise generation, and high noise immunity where as MIPI C-PHY℠ was designed to coexist with MIPI D-PHY℠ on the same IC pins , allowing dual-mode devices to be produced.

Arasan has been a member of MIPI for over ten years. We are active participants in several working groups. We work closely with other member customers to ensure compliant implementation of standards-based IP. Arasan's innovatively worked on the development of a MIPI C-PHY℠/D-PHY℠ combo PHY that is complaint with the latest MIPI C-PHY℠ v2.0 and MIPI D-PHY℠ v2.5.

# MIPI C-PHY℠

The MIPI C-PHY℠ interface is a modern synchronous digital networking bus for applications such as smartphones, augmented reality headsets and the Internet of Things platforms, which is usable in high-speed, low-speed applications. The MIPI C-PHY℠ norm creates a generic solution for transferring data with high throughput per physical conductor, which makes the device very special in contrast with conventional wireless buses. In addition to circuit-level strategies and concerns for applying this revolutionary scheme, the principle of three-phased encoding has been implemented, along with higher mapping criteria and some ramifications for protocol levels, including fast clock recovery and effective sideband signaling for unmapped terms. With this realization, MIPI C-PHY℠ is the embodiment of an evolving digital bus class conventional signal, that incorporates the advantage of single-ended and differential signals in order to retain a low pin count without losing electromagnetic noise immunity.

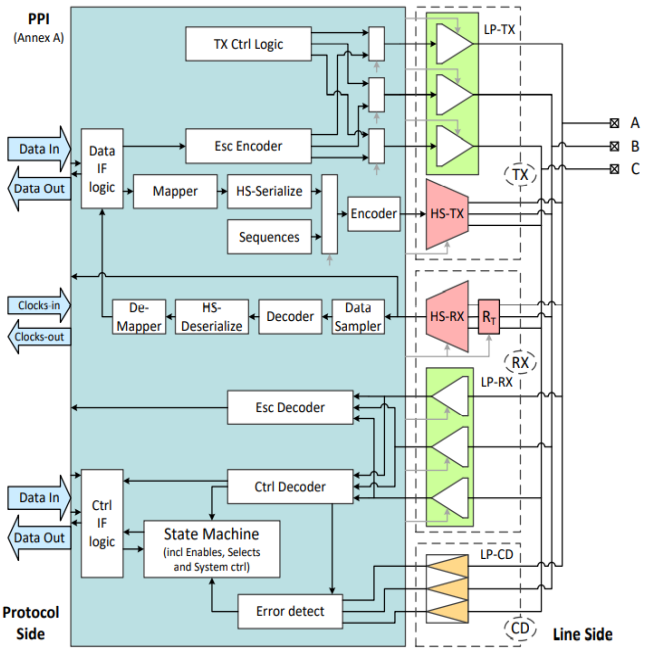


**Figure: MIPI C-PHY℠ Block Diagram**

Arasan's MIPI C-PHY℠ IP Core is fully compliant to the MIPI C-PHY℠ specification Version 1.2 while also being compliant to the D-PHY℠ 1.2 Specification. It supports the MIPI® Camera Serial Interface (CSI-2) and Display

Serial Interface (DSI-2) protocols. It is a universal PHY that can be configured as a transmitter, receiver or both. This IP core is specially optimized for area and power. The MIPI C-PHY℠ is targeted toward high resolution displays to more efficiently transfer data with lower power consumption and die size compared to the D-PHY℠. It utilizes a lower signal rate than the MIPI D-PHY℠ but provides support for low-cost, low-resolution image sensors, sensors offering up to 60 megapixels; and 4K video display panels.

Arasan's MIPI C-PHY℠ v1.2 achieves a peak bandwidth of 3.5 Gb/s at 2.28 bits/symbol, or 17.1 Gbps over a 9-wire interface, compared to the MIPI D-PHY℠ v1.2 peak transmission rate of 2.5 Gbps/lane or 6 Gbps over a 10 wire - 4 lane interface.

Arasan's MIPI C-PHY℠ is immediately available for the TSMC 22nm and below which is verified, and silicon proven for Arasan Total IP™ for MIPI camera interface CSI-2® and MIPI display interface DSI® and DSI-2®. Arasan's MIPI C-PHY℠ is also available in 28nm and 16nm, 12nm processes.

Arasan's MIPI C-PHY℠ is compliant to the MIPI's latest C-PHY℠ and key features are as below:

- Supports standard PHY transceiver compliant to MIPI Specification.
- Supports standard PPI interface compliant to MIPI Specification.
- Supports asynchronous transfer at high speed mode with a symbols rate of 80-2500 MS/s.
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s.
- Spaced one hot encoding for Low power [LP] data.
- Supports maximum of three data lanes.
- Supports error detection mechanism for sequence errors and contentions.
- Data lanes support transfer of data in high speed mode.
- Supports ultra-low power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PPI.
- Activates and disconnects high speed terminators for reception and transmission.
- On-chip clock generation configurable for transmitter.

# MIPI D-PHY℠

MIPI D-PHY℠ binds high-resolution cameras and screens to a processor. It's a synchronous clock-forwarded connection with high immunity to noise and a high resistance. MIPI D-PHY℠ makes low latency switches between low and high-speed modes.

Since it offers a flexible, high-speed, low-power and low-cost solution, it is an in demand PHY for cameras and displays on smartphones. It is also used in many other uses, including helicopters, large smartphones, surveillance cameras and industrial robotics. MIPI D-PHY℠ is still used extensively in vehicle applications with the help of patented bridging solutions, including camera sensing devices, radar collision prevention, in-car infotainment and dashboards.

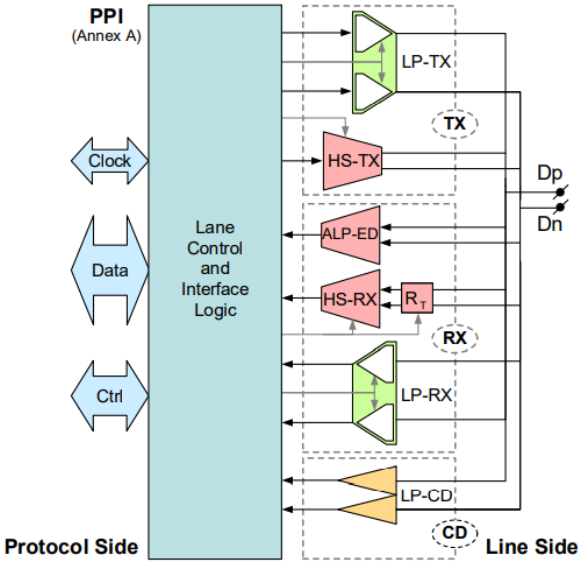


**Figure: MIPI D-PHY℠ Lane Diagram**

Due to the master-slave relationship of the connection transceivers, service and data rates required for a link are asymmetrical. For the monitor and camera use cases with one main data transmitting path, the asymmetric architecture greatly reduces the difficulty of the connection. The operation is optional, bi-directional and half-duplex.

At Arasan Chip Systems, MIPI D-PHY℠ v1.1 IP with supporting speed of up to 1.5 Gbps and MIPI D-PHY℠ v1.2 IP with supporting speed of up to 2.5 Gbps, is available immediately for the TSMC 22nm and below process technology. The

MIPI D-PHY℠ IP is further optimized for lower power targeting wearables and IoT Display applications which require low throughput for their small lower resolution screens, but where power is of paramount importance.

The MIPI D-PHY℠ IP is also available as a Tx only IP for companies looking to save silicon area and further improve power consumption. The MIPI D-PHY℠ IP on TSMC 22nm is seamlessly integrated and verified with Arasan's own MIPI DSI℠ Tx and MIPI DSI℠ Rx IP cores as part of its Total IP™ MIPI Display interface for wearables and IoT.

Arasan's MIPI D-PHY℠ is compliant with the latest MIPI D-PHY℠ specs, possessing the following key features:

- Supports D-PHY 1.1 synchronous transfer mode at high speed mode with a bit rate of 80-1500 Mb/s without deskew calibration.
- Supports DPHY 1.2 for 1500 – 2500 Mb/s with deskew calibration.
- Supports DPHY 2.1 for 2500 – 4500 Mb/s with deskew calibration.
- Asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data.
- One clock lane and four data lanes
- On-chip clock generation configurable for either transmitter or a receiver
- On-chip clock generation configurable for either receiver
- Data lanes support transfer of data in high speed mode.
- Features include ultralow power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data transmission from and to the PPI.
- Supports standard PHY receiver and PPI interface compliant to MIPI Specification.
- Testability for Analog Rx with DLL and DFE.
- Supports High speed mode in Forward communication and for Stuck-At Scan for Digital Testing
- Runs off 0.8V+/-10%, 1.2V+/-10%, 1.8V +/- 10% supply.
- Has inbuilt calibration to calibrate RX impedance. Also, can manipulate those impedance manually through trim registers.
- Supports polarity swap.

# MIPI C-PHY℠ v2.0 + D-PHY℠ v2.5 Combo IP Core

Arasan's latest MIPI C/D-PHY Combo IP complies with the MIPI Alliance C-PHY℠ v2.0 and D-PHY℠ v2.5 specifications, with world class area and power dissipation, and is available for a range of foundry processes. This IP delivers 6 Gbps per lane for a max throughput of 24 Gbps in D-PHY℠ mode, and 6 Gsps per trio for a max throughput of 41.04 Gbps in C-PHY℠ mode. The C/D-PHY IP interfaces seamlessly to both D-PHY℠ and C-PHY℠ based sensors over its MIPI CSI-2® IP Core and MIPI Displays that are increasingly adopting C-PHY over our MIPI DSI-2℠ IP core.

This combo PHY provides a low-power and high-performance interface for platforms ranging from processors to peripheral devices for mobile, automotive, AI and IoT applications. It inter-operates seamlessly with Arasan Chip Systems CSI-2® and DSI-2℠ and offers built-in test capabilities including PRBS generator and internal loopback to support cost effective tests for high volume manufacturing.

This combo PHY may be configured as either a D-PHY℠ with one clock and up to four data lanes, or a C-PHY℠ with up to 3 trio lanes. Area overhead to support both modes is minimized by reusing the D-PHY℠ blocks and high-speed IO's.

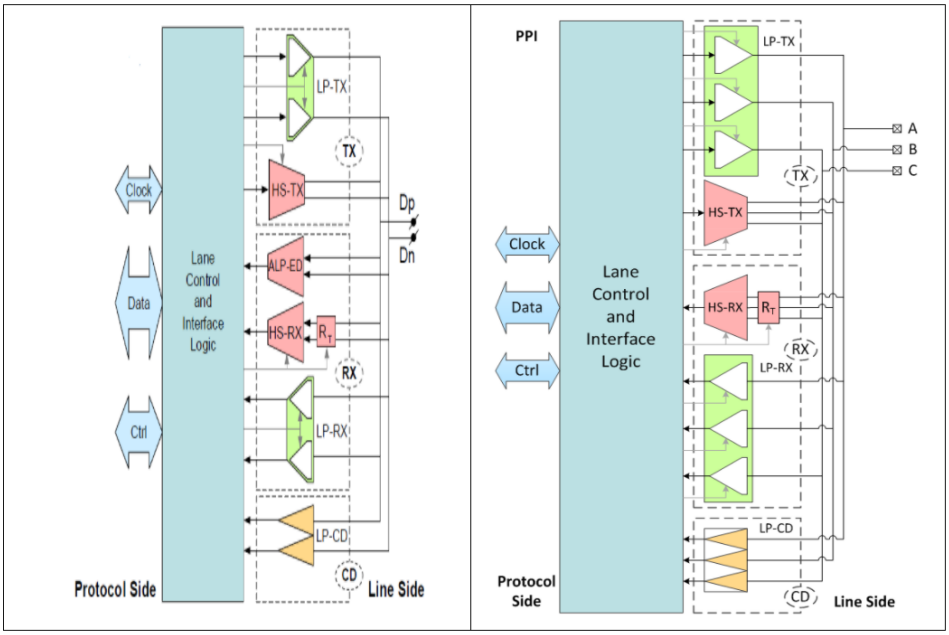


**Figure: Arasan's MIPI C-PHY℠/D-PHY℠ Combo**

**Key Features**

- When used with Arasan's MIPI CSI-2® or MIPI DSI-2®, the MIPI C-PHY℠/D-PHY℠ combo IP offers built-in test capabilities including PRBS generator and internal loopback to support cost effective tests for high volume manufacturing.
- New power saving HS-Tx half swing mode for D-PHY℠,
- On-board programmable PLL with Spread Spectrum Clocking, with or without deskew calibrations and equalization for different operating speeds of D-PHY℠, Power management functions such as reduced HS-TX swing modes and unterminated HS-RX mode.
- It supports ALP Mode for different applications with long channels that t enables fast lane turnaround mode to increase bandwidth of communication in the reverse direction of the MIPI link. The ALP mode is key to the CSI-2® Unified Serial Linking capability, which decreases interface wires and helps to allow a more extensive range.

For a detailed comparison of MIPI C-PHY℠ and MIPI D-PHY℠ please see below link.

White Paper - Arasan's MIPI C-PHY℠ vs MIPI D-PHY℠