MIPI C-PHY℠ v2.0 + D-PHY℠ v2.5 Combo IP Core

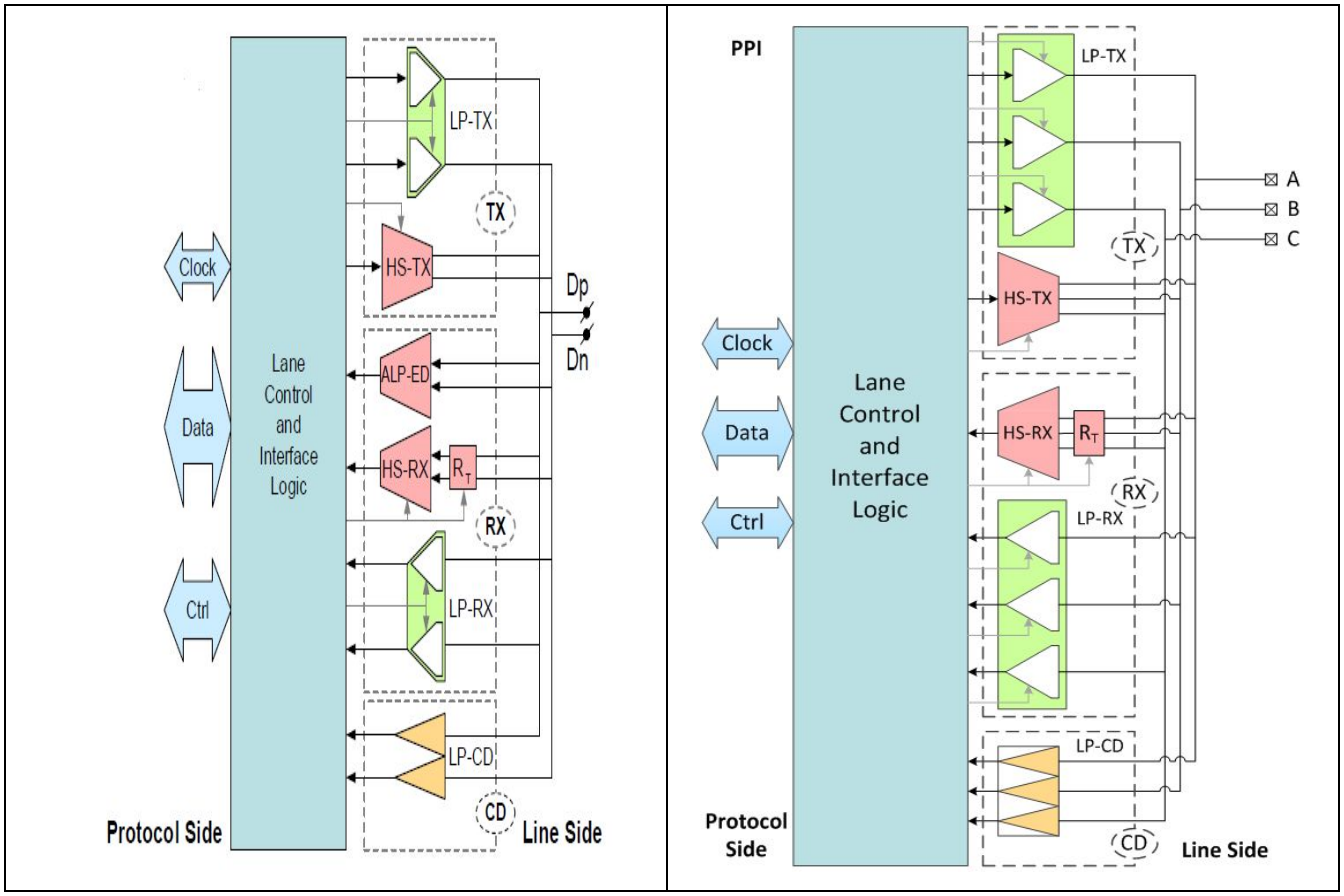
Overview

Arasan Chip Systems, the leading provider of IP for MIPI Standards, presents its latest MIPI C/D-PHY Combo IP. This Tx/Rx transceiver complies with the MIPI Alliance C-PHY℠ v2.0 and D-PHY℠ v2.5 specifications, with world class area and power dissipation, and is available for a range of foundry processes. This IP delivers 6 Gbps per lane for a max throughput of 24 Gbps in D-PHY℠ mode, and 6 Gsps per trio for a max throughput of 41.04 Gbps in C-PHY℠ mode. The C/D-PHY IP interfaces seamlessly to both D-PHY℠ and C-PHY℠ based sensors over it's MIPI CSI-2® IP Core and MIPI Displays that are increasingly adopting C-PHY over our MIPI DSI-2℠ IP core.

This combo PHY provides a low-power and high performance interface for platforms ranging from processors to peripheral devices for mobile, automotive, AI and IoT applications. It inter-operates seamlessly with Arasan Chip Systems CSI-2® and DSI-2℠, and offers built-in test capabilities including PRBS generator and internal loopback to support cost effective tests for high volume manufacturing.

This combo PHY may be configured as either a D-PHY℠ with one clock and up to four data lanes, or a C-PHY℠ with up to 3 trio lanes. Area overhead to support both modes is minimized by reusing the D-PHY℠ blocks and high-speed IO's.

Diagrams



Key Features

- 4-lane D-PHY℠ 2.5 provides:
  - 18 Gbps when operating at 4.5 Gbps
  - 24 Gbps when operating at 6.0 Gbps
- 3-channel C-PHY℠ 2.0 provides:
  - 30.78 Gbps when operating at 4.5 Gsps
  - 41.04 Gbps when operating at 6.0 Gsps (provides 13.68 Gbps per trio per lane)
- Supports HS, LP, ALP and CD modes
- Supports Fast lane Turnaround mode, low-power escape modes and ultra low-power state modes
- 80 Mbps to 1.5 Gbps per data lane in D-PHY℠ mode without deskew calibration
- Up to 2.5 Gbps per data lane in D-PHY℠ mode with deskew calibration
- Up to 4.5 Gbps per data lane in D-PHY℠ mode with equalization
- Up to 4.5Gsps (10.26 Gbps) per data trio-lane in C-PHY℠ mode available "off the shelf" for process nodes 28nm & 22nm.
- Full 6 Gbps for D-PHY optionally available on all process nodes 12nm and below.
- Full 6 Gsps for C-PHY optionally available on all process nodes 12nm and below.
- On-board programmable PLL with Spread Spectrum Clocking
- New power saving HS-Tx half swing mode for D-PHY℠
- Supports HS-IDLE mode for D-PHY℠
- Supports HS Deskew, Alternate calibration sequence, Preamble sequence
- Support HS Reverse
- Supports polarity swap for all lanes between DP/DN or A/B/C
- SPI register access to all registers
- Supports standard PPI interface compliant with MIPI Specifications
- Activates and disconnects high speed termination for Rx and Tx modes
- "Support for Stuck-At scan" for DC scan feature.
- Total IP™ for MIPI Imaging & Display Interface from Arasan
  - Seamlessly integrated with Arasan's CSI-2® and DSI-2℠ Digital Controller IP which support C-PHY v2.0 and D-PHY v2.5 features and the maximum throughput with low overhead loss.
  - Limited availability of Test Chips (on TSMC FINFET) and HDK from Arasan.

Deliverables

- GDS-II Database
- LVS Netlist
- Physical Abstract Models (LEF)
- Timing Models (LIB)
- Process Specific Integration Guide
- User Guide
- Customer support