Arasan MIPI® CSI-2-RX IP Verification Using Questa® VIPs

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This article describes the verification process of the ARASAN MIPI® CSI-2-RX IP core using Questa® VIPs by Mentor, A Siemens Business.

MIPI CSI-2 PROTOCOL

MIPI Camera Serial Interface 2 (CSI-2) provides an interface between a peripheral device (such as a camera module) and a host processor (such as a baseband or application engine). It is mostly used in the mobile and automotive industries. High performance and low power are the key features of this protocol.

MIPI CSI-2 provides two high-speed serial data transmission interface options. The first option, which is referred to as the D-PHY physical layer option, uses a differential interface with one 2-wire clock lane and one or more 2-wire data lanes. The second high-speed data transmission interface option, which is referred to as the C-PHY physical layer option, uses one or more unidirectional 3-wire serial data lanes, each of which has its own embedded clock.

ARASAN MIPI CSI-2 RECEIVER IP

The Arasan MIPI CSI-2 Receiver IP provides a standard, scalable, low-power, and high-speed interface that supports a wide range of high image resolutions. It is compliant with the MIPI CSI-2 v1.3 specification and supports D-PHY v1.2 and MIPI C-PHY v1.1.

Arasan offers C-PHY in a combination configuration that supports both the C-PHY interfaces and the D-PHY interfaces. This IP connects to D-PHY or C-PHY through the PHY-Protocol Interface (PPI) interface that is compliant to the D-PHY and C-PHY specifications. Most of the PPI signals are common for D-PHY and C-PHY except for a few additional signals in each mode. The usage of PHYs is selected by simple programming based on the use case.

Arasan CSI-2 Rx IP, CSI-2 Tx IP, D-PHY IP, and C-PHY IP are silicon-proven and currently used in MIPI Protocol Analyzers and Production Test Applications. Mentor Questa® VIP further enhances Arasan IP compliance to the MIPI Specifications, enabling the IP to meet the stringent requirement of compliance test applications.

The following are the key features of the Arasan MIPI CSI-2 Receiver IP:

- Use of either D-PHY or C-PHY through user configuration
- 4-Lanes or 8-Lanes D-PHY, and 3-Lanes C-PHY
- Supports for Ultra-Low Power Mode (ULPS)
- Supports for Alternate Low Power State (ALPS) in C-PHY mode
- Single (or) Optional Multi-Pixel mode interface to ISP

Multi-Pixel mode is used in high bandwidth requirement applications to lower the ISP clock frequency requirement.

- Optional Pixel Level Interface to ISP with HSYNC, VSYNC, DATA, and DATA VALID
- Streams the received pixels onto eight data channels (customizable) based on the channel configuration from ISP
- Separate data channel for short generic packets
- Support for all packet level errors, Protocol Decoding Level errors
- Pixel formats supported:
  - RAW data type – RAW6, RAW7, RAW8, RAW10, RAW12, RAW14, RAW16, RAW20
  - YUV data type – YUV422-8bit, YUV422-10bit, Legacy YUV420 8-bit, YUV420 10-bit, YUV420 8-bit (Chroma Shifted Pixel Sampling), YUV420 10-bit (Chroma Shifted Pixel Sampling)
  - RGB data type – RGB888, RGB666, RGB565, RGB555, RGB444
  - All user Defined data types / JPEG
  - Generic 8-bit long packet data types

- Capability for programming both CSI-2 and PHY-related registers Reserved address space [0x00-0x0F] for the PHY-related registers
- Host interface for register configuration and monitoring
- Optional support for the AHB or APB interface

SYSTEM ARCHITECTURE

There are two mutually exclusive modes of operation (Register configurable), Mode-0 (D-PHY) and Mode-1 (C-PHY). Both modes use common PPI interface signals and some additional signals that are unique to each mode, as shown in figure 1.

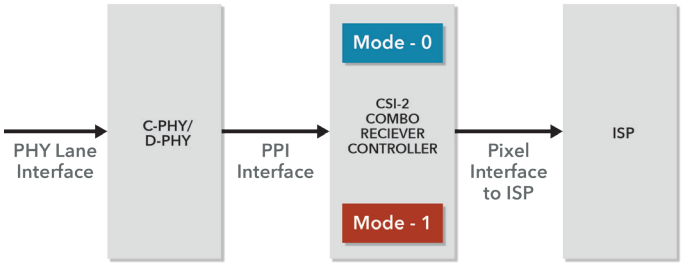

Figure 1

FUNCTIONAL BLOCKS

The CSI-2 Receiver IP is partitioned into sub-modules to accomplish the required functionality with the following units, as shown below in figure 2:

- APB Target Interface
- Lane Merger Layer Unit
- Low-Level Protocol Unit
- FIFO (External)
- Byte to Pixel Unit
- Image Processor Interface Unit
- MIPI Interface

CSI-2 QUESTA VERIFICATION IP

The CSI-2 Questa® Verification IP (CSI-2 QVIP) is a comprehensive verification IP built using advanced methodologies with advanced debug, coverage, and protocol checking for the fastest time-to-verification sign-off. The following are the key features of the CSI-2 QVIP:

- Fully compliant with UVM Standard
- Compatible with all popular industry simulators

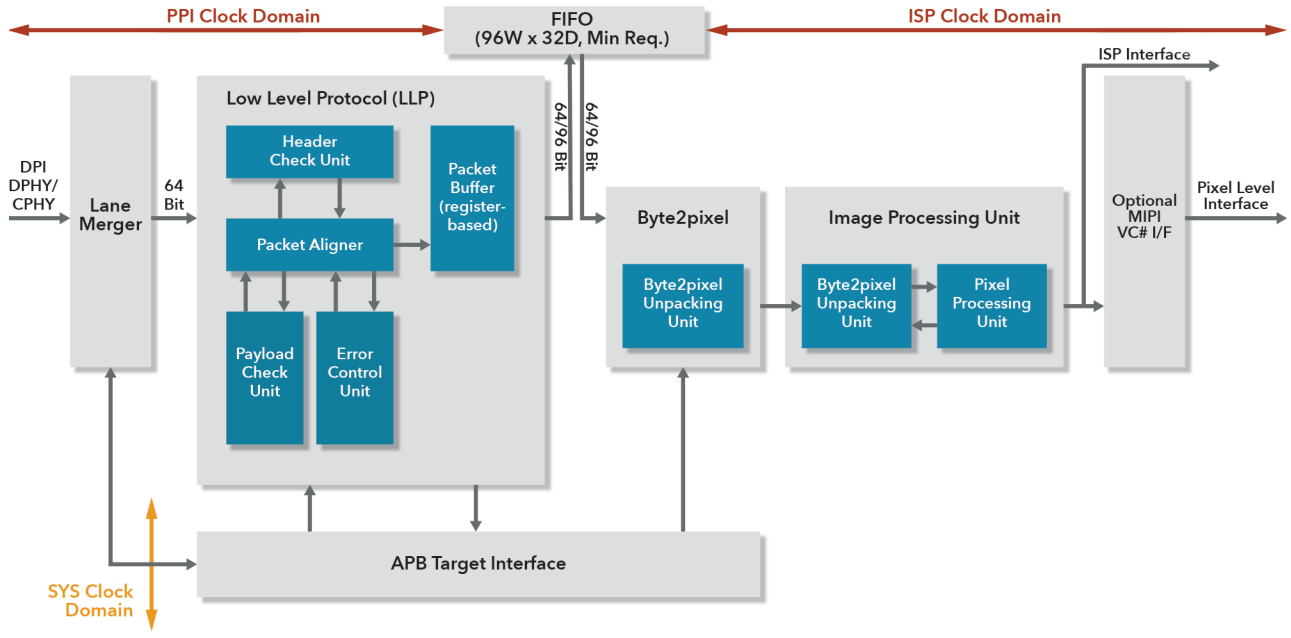

Figure 2

- Unencrypted Test Sequence Library
- Verification Plans and Coverage

The CSI-2 QVIP consists of a UVM agent that has been configured with an active slave PPI peripheral camera settings. This UVM agent has both the Driver and the Monitor that drive and monitor the slave PPI interface, respectively, as shown below in figure 3.

- CSI-2 QVIP driver
  - o Drives scheduled sequence items over the PPI interface
- CSI-2 QVIP monitor
  - o Collects CSI-2 packets from the PPI interface
  - o Monitors protocol compliance checking with assertions
  - o Sends packet to the scoreboard for checking
  - o Samples coverage measuring the percentage of verification objectives
- CSI-2 QVIP Scoreboard
  - o Predicts packets with configured settings
  - o Flags UVM_ERROR for any mismatch between the predicted and the observed packet

VERIFICATION USING MIPI CSI-2 QVIP

The testbench verification environment is developed using the SystemVerilog language and is aligned with UVM-1.2. The CSI-2 QVIP used in the testbench environment is developed by Mentor, A Siemens Business. Some of the testbench components are part of the CSI-2 QVIP package and all the other components have been developed from scratch.

- CSI-2 IP Pixel Interface - SystemVerilog virtual interface for accessing CSI-2 IP pixel-level interface signals
- CSI-2 IP Monitor - UVM monitor converting signal-level activity into TLM transactions and broadcasts the packets from the CSI-2 IP pixel interface
- CSI-2 Scoreboard - Comparing packets from the CSI-2 IP monitor and the CSI-2 QVIP monitor

The UVM testbench below starts with DUT bring up and configurations, which are done using APB and AHB sequences. Once the configuration phase is complete, the tests start a camera sequence to generate various frames from the CSI-2 QVIP.

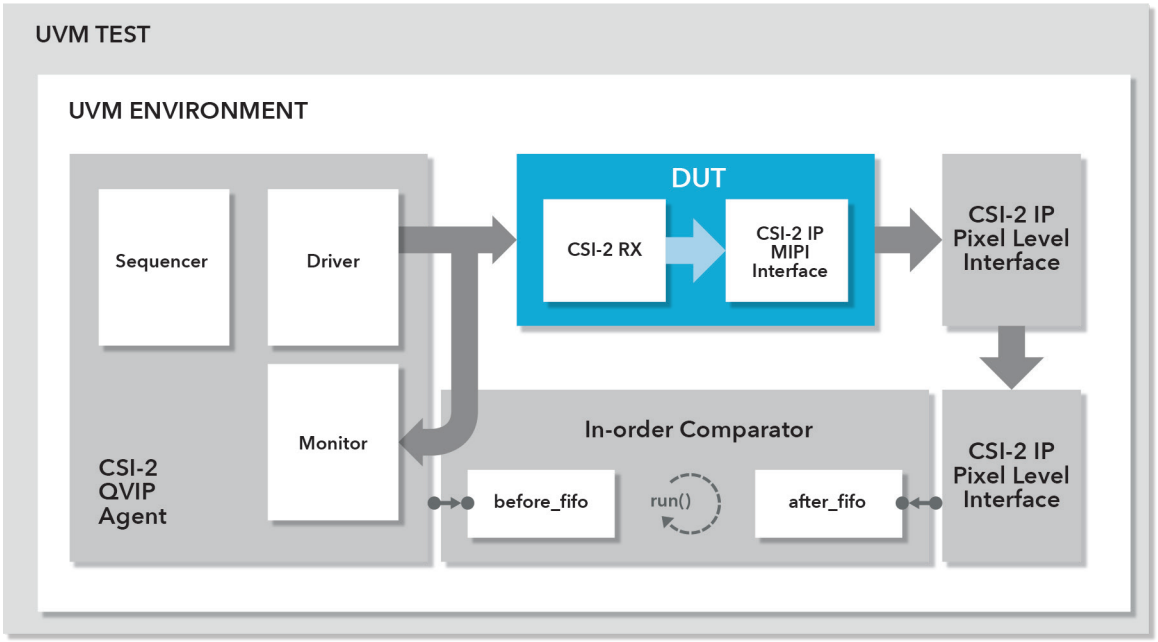

Figure 3

The sequences used are based on constraint-driven stimulus generation, which allows users to automatically generate the necessary stimulus for functional verification. Random testing can be more effective than a traditional, directed testing approach because it can generate corner-case scenarios that would otherwise be missed. It represents an effective method to achieve the coverage goals quickly and with a low number of tests.

The CSI-2 QVIP sequencer takes the sequence item from the CSI-2 QVIP sequences and passes them to its driver, which translates them to the CSI-2 PPI interface. The CSI-2 QVIP in-built monitor collects all packets and sends them to the scoreboard. The CSI-2 QVIP monitor also provides protocol assertions validating the DUT behavior over PPI Interface. The scoreboard class contains two analysis FIFOs and two analysis exports. One of them is connected to the CSI-2 QVIP monitor and another one is connected to the CSI-2 IP monitor. All monitored CSI-2 packets are stored in a scoreboard FIFOs and are compared.

CONCLUSION

The MIPI CSI-2 Questa® Verification IP is highly configurable and is aimed for ease of use through advanced verification methodologies. A large library of standard SystemVerilog UVM components with consistent common architecture is used in this VIP. It includes test plans, compliance tests, test sequences, protocol coverage in SystemVerilog and XML source code, a comprehensive set of protocol checks, error injection, and debug capabilities. These features ensure rapid deployment within a verification team and easy reuse, extension, and debug capabilities.

Questa® Verification IP, powered by its flexible architecture, integrates seamlessly into advanced verification environments, including testbenches built using UVM, Verilog, VHDL, and System-C. It is the industry's only VIP with a native SystemVerilog UVM architecture across all protocols, ensuring maximum productivity and flexibility. In addition, comprehensive protocol assertions of the VIP solution allow Questa® Formal users to exhaustively prove design correctness.

Mentor Questa® Verification IP is an integral part of the Enterprise Verification Platform™ (EVP). Together with the Questa® Verification Solution, VIP components reduce bring up time and enable rapid coverage closure.

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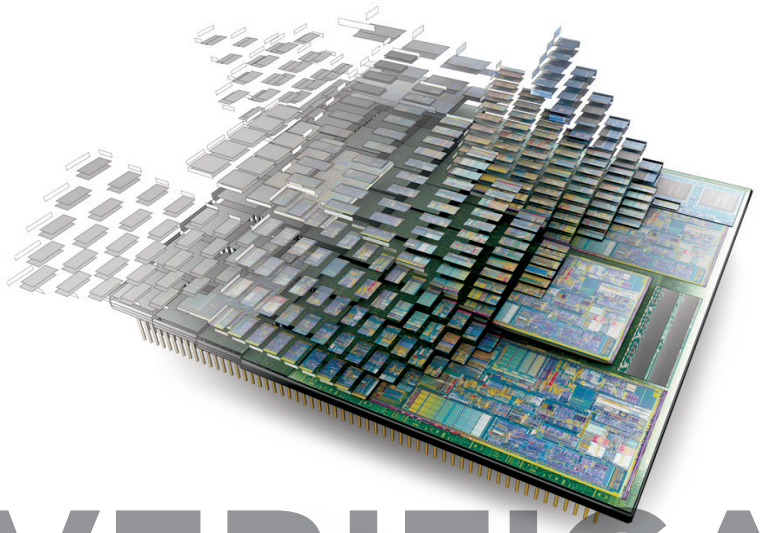

VERIFICATION HORIZONS

VH