MIPI I3C PHY

Revision1. 2

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1 Introduction

1.1 About MIPI I3C

The I3C bus is used for various sensors in the mobile/automotive system where the Host transfers data and control between itself and various sensor devices. The I3C interface is intended to improve upon the features of the I2C interface, preserving backward compatibility. This I3C defines a standard multi-Drop interface between Host processors and peripheral Devices (e.g., sensors). Implementing the I3C Specification greatly increases the flexibility system designers have to supplant incumbent interfaces (i.e., I2C, SPI, UART) and support a wide array of Devices of increasing complexity and diversity in their system (e.g., sensor subsystem) and at as low a cost as possible.

1.2 Arasan's Contribution to MIPI

Arasan has been a member of MIPI for over ten years. We are active participants in several working groups. We work closely with other member customers to ensure compliant implementation of standards-based IP.

1.3 Arasan's Total IP™ Solution

Arasan provides a Total IP™ Solution, which encompasses all aspects of IP development and integration, including analog and digital IP cores, verification IP, software stacks & drivers, and hardware validation platforms. Benefits of Total IP™ Solution:

- Seamless integration from PHY to Software
- Assured compliance across all components.
- Single point of support
- Easiest acquisition process (one licensing source)
- Lowest overall cost including cost of integration.
- Lowest risk for fast time to market.

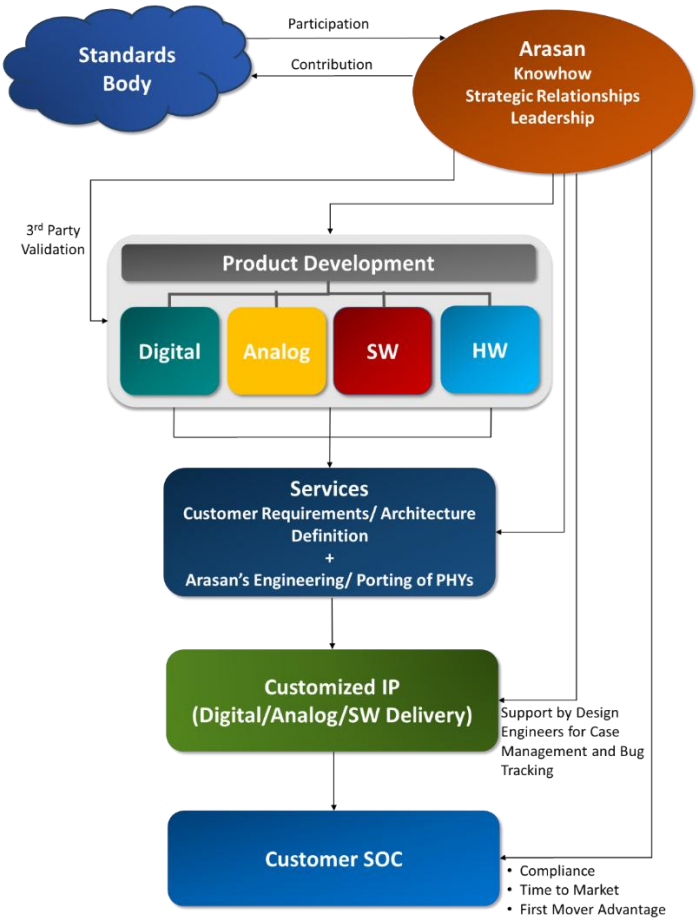

Figure 1Arasan's Total IP™ Solution

2 Arasan's MIPI I3C PHY

2.1 Arasan's MIPI I3C Host PHY

2.1.1 Features

- Compliant with MIPI specification for I3C v1.1
- Supports DC operating parameters of both the modes: Open-drain & Push-Pull
- Higher speeds are achieved in Push-Pull mode using a totem pole driver in SDA
- Supports 1.8V/1.2 +/-10% supply for IOs and 0.8V +/-10% supply for the core.

2.1.2 Architecture

Figure below shows the block diagram of Arasan's MIPI I3C Host PHY and the Figure shows the Host PHY in detail.

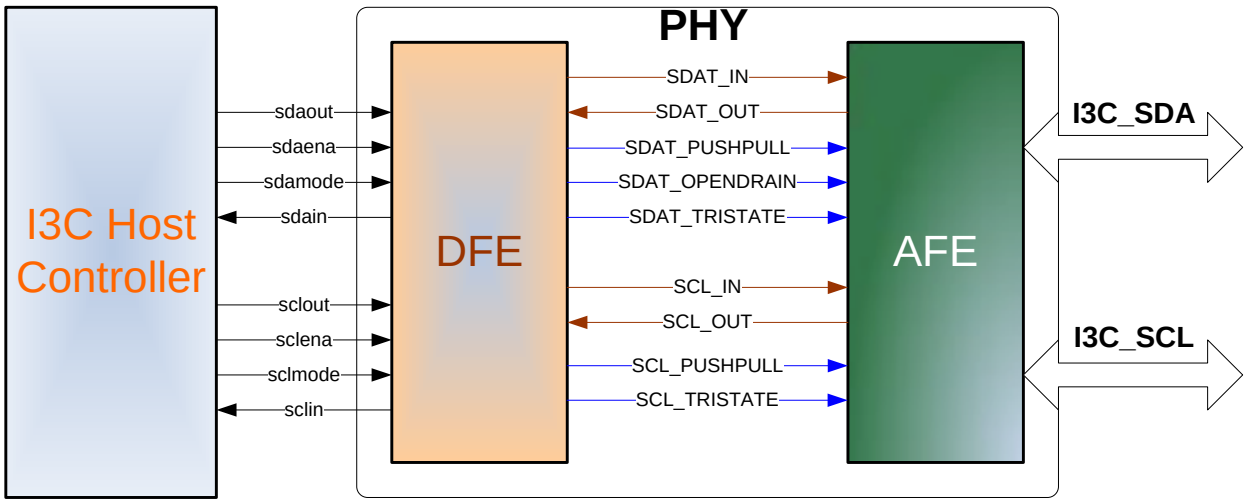

Figure 2 Arasan's MIPI I3C Host PHY Block Diagram

2.1.3 PIN List

PIN	Direction	Description
Interface between Controller/DFE (controller side IN and OUT)		
sdaout	OUT	This is the output for the SDA Pin
sdaena	OUT	This is the SDA control line enable
sdamode	OUT	SDA Mode. 0: Open-Drain, 1-Push-pull
sdain	IN	This is the input from the SDA Pin
sclout	OUT	This is the output for the SCL Pin.
sclena	OUT	This is the SCL control line Enable
sclmode	OUT	SCL Mode. 0: Open-Drain, 1-Push-pull
sclin	IN	This is the clock from the SCL pin
Interface between DFE/AFE (AFE side IN and OUT)		
sdat_in	IN	Incoming data on SDA
sdat_out	OUT	Outgoing data on SDA
sdat_OD	IN	Active High signal indicates the SDA pad Open Drain operation
sdat_trist	IN	Active high signal indicates the SDA pad tri state
scl_in	IN	Incoming Clock
scl_out	OUT	SCL Clock out
AFE Output		
I3C_SDAT	INOUT	Bi-directional SDA – Data Lane
I3C_SCL	INOUT	Bi-directional SCL – Clock Lane

2.1.4 Power pins

No	Pins	Dir	Description
1	VDDIO	IO	Analog IO power pins
2	VCORE	I	Analog Core power pins
3	GNDC	I	Analog Core ground pins
4	VSSQ	IO	Analog IO ground pins

2.2 Arasan's MIPI I3C Device PHY

2.2.1 Features

- Compliant with MIPI specification for I3C v1.1
- Supports DC operating parameters of both the modes: Open-drain & Push-Pull
- Higher speeds are achieved in Push-Pull mode using a totem pole driver in SDA
- Supports 1.8V/1.2 +/-10% supply for IOs and 0.8V +/-10% supply for the core.

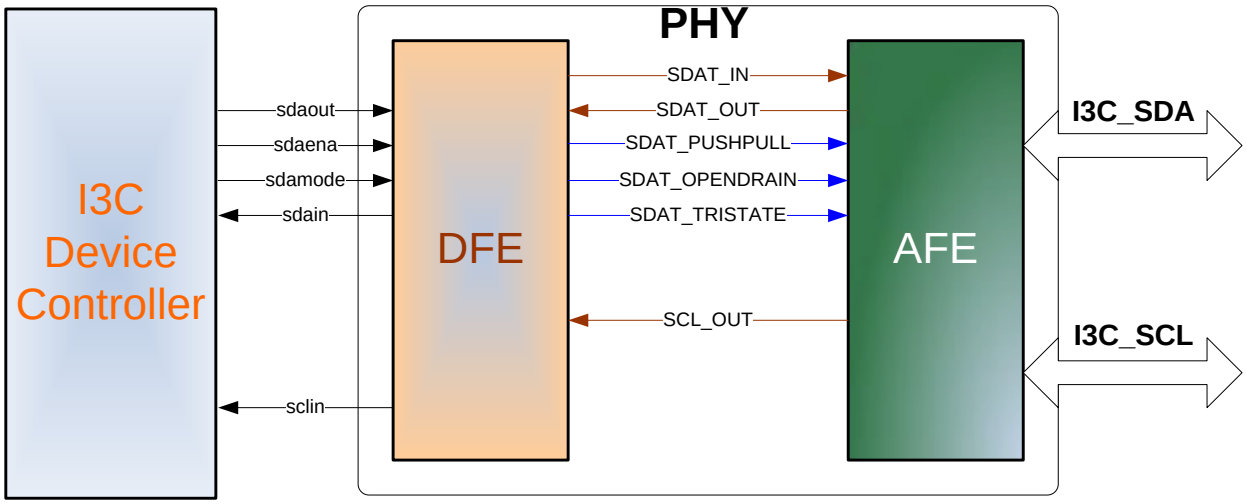

Figure 3 Arasan's MIPI I3C Device PHY Block Diagram

2.3 SOC Level Integration

2.3.1 IP Deliverables

- GDSII
- CDL netlist for LVS
- LIB files
- LEF files
- Scan-inserted netlist with test guide
- Behavioral model with verification environment
- DRC and antenna reports
- Design integration guide
- User guide