Datasheet

Total MIPI Camera IP Solution

CSI-2 v1.3 Transmitter Controller
CSI-2 v1.3 Receiver Controller
C-PHY v1.1 Physical Interface
D-PHY v1.2 Physical Interface

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1 Introduction

1.1 About CSI

The MIPI®Alliance the Camera Serial Interface (CSI-2) dates back to November 2005 and was in widespread use in consumer devices by 2009. CSI-2 V1.1 was approved in January 2013. CSI-2 v1.2 was released in September 2014. The updated version, CSI-2 v1.3 (covered in this document) was released in February 2015.

Demand for increasingly higher image resolutions is pushing the bandwidth capacity of existing host processor-to-camera sensor interfaces. Common parallel interfaces are difficult to expand, require many interconnects and consume relatively large amounts of power. Emerging serial interfaces address many of the shortcomings of parallel interfaces while introducing their own problems. Incompatible, proprietary interfaces prevent devices from different manufacturers from working together. This can raise system costs and reduce system reliability by requiring “hacks” to force the devices to interoperate. The lack of a clear industry standard can slow innovation and inhibit new product market entry.

CSI-2 provides the mobile industry a standard, robust, scalable, low-power, high-speed, cost-effective interface that supports a wide range of imaging solutions for mobile devices.

1.2 Arasan’s Contribution to MIPI

Arasan has been a member of MIPI for over ten years. We are active participants in a number of working groups. We work closely with other member customers to ensure compliant implementation of standards based IP.

1.3 Arasan’s Total IP Solution

Arasan provides a Total IP Solution, which encompasses all aspects of IP development and integration, including analog and digital IP cores, verification IP, software stacks & drivers, and hardware validation platforms. Benefits of Total IP Solution:

- Seamless integration from PHY to Software
- Assured compliance across all components
- Single point of support
- Easiest acquisition process (one licensing source)
- Lowest overall cost including cost of integration
- Lowest risk for fast time to market

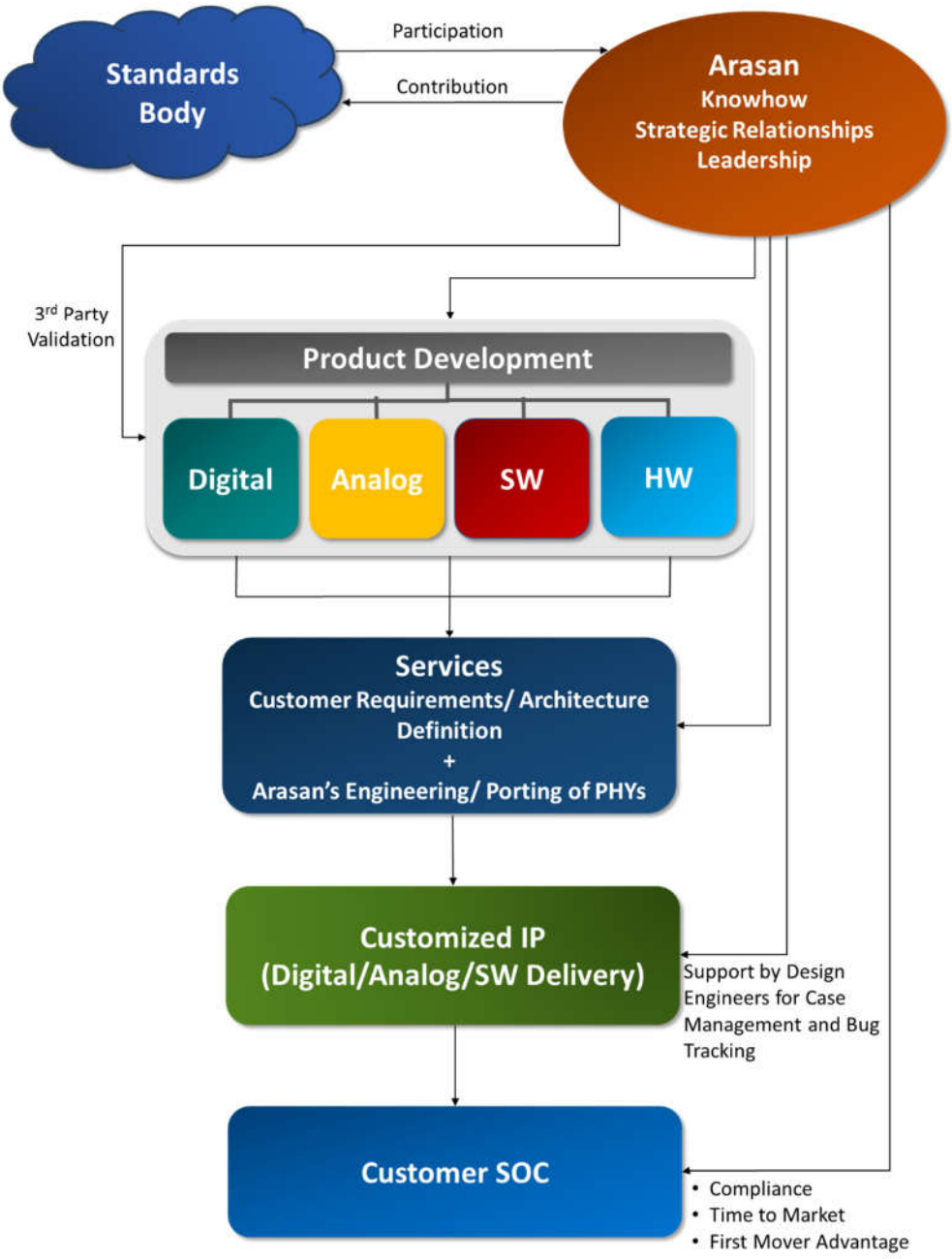


Figure 1: Arasan's Total IP Solution

2 CSI-2 v1.3 Transmitter IP

2.1 Overview

Arasan Chip Systems is a leading SOC IP provider of a complete suite of MIPI compliant IP solutions, which consist of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms for software development and compliance testing, and optional customization services.

The MIPI compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Arasan IP Core that functions as a MIPI CSI-2 Transmitter, which typically resides in a mobile platform's camera module, and communicates over a D-PHY/C-PHY link to a CSI2 Receiver in the applications processor. The Arasan CSI-2 combo IP is MIPI-compliant and provides a standard, scalable, low-power, high-speed interface that supports a wide range of higher image resolutions.

2.2 Features

- Compliant with the following MIPI specifications:
  - mipi_CSI-2_specification_v1-3
  - mipi_CSI-2_specification_v1-2
  - mipi_D-PHY_specification_v1-2
  - mipi_C-PHY_specification_v1-0

- CSI-2 Combo Transmitter Core features:
  - Use of either D-PHY/C-PHY by user configuration
  - Lane Configurability depending on the bandwidth requirements of the application, up to 8-lanes for DPHY and up to 4-lanes for C-PHY
  - Connectivity to DPHY/CPHY through MIPI PPI Interface
  - High Speed (HS) transmit rates of 182Mbps to 5714Mbps per lane with C-PHY interface
  - High Speed (HS) transmit rates of 40Mbps to 2500Mbps per lane with D-PHY interface
  - Support for Ultra Low Power Mode (ULPS)
  - Support for Continuous and Non-Continuous Clock Mode

  - Pixel formats supported
    - RAW data type
    - YUV data type
    - RGB data type
    - All user Defined data types / JPEG
    - Generic 8-bit long packet data types

- Supports Data Type Interleaving
- Supports Virtual Channel Interleaving
- Pixel Level Input Interface for Image Sensor
- Supports Header and Payload Checksum
- Configurable for two mode of operation
    - Store and Forward Mode – Stores the full pixel packet before forwarding.
    - Cut through Mode – Initiates the HS transmission to D/CPHY as soon as the pixel information is received. Makes use of very shallow memory.
- Supports Multi Pixel Mode – Multiple Pixels per clock to bring down the sensor clock frequency to support higher resolution applications
- PPI Data Lane swapping as per user configuration
- Optional support for Compressed data formats

- Host interface for register configuration and monitoring,
    - Used for programming both CSI-2 and PHY related registers. Reserved address space [0x00 – 0x0F] for the PHY related registers.
    - Optional support for the AHB/APB/Microcontroller Interface

2.3 Architecture

2.3.1 Functional Description

The Arasan CSI-2 Transmitter IP is designed to provide MIPI CSI-2 v1-2/ CSI-2 v1-3 compliant high speed serial connectivity for camera modules in mobile platforms. Serial connectivity between this IP to the mobile applications processor's CSI-2 Receiver is implemented using 1 to 8 D-PHY Lanes (or) 1 to 6 C-PHY lanes, depending on camera sensor resolutions and the resulting bandwidth needs. This IP connects to the D-PHY/CPHY through the PPI interface. The PPI interface of the IP is compliant to MIPI mipi_D-PHY_specification_v1-2/mipi_C-PHY_specification_v1-0. The usage of PHY's is selected by simple programming based on the use case.

Initial configuration of this IP and its associated D-PHY/C-PHY can be done through programmed IO over an AHB/APB bus. However, other bus interface can be provided upon request.

Pixel Data received from over the Camera Sensor Bus is packed into bytes by the Transmitter IP. The packing of the pixel into bytes follows the CSI-2 spec and based on the pixel format support. This IP calculated and appends an ECC/CRC value to a short packet (or) to the header of a long packet. Selection of ECC/CRC to the header is done based on the PHY connected. For the payload of a long packet carrying pixel data, this IP calculates its CRC value and appends to the packet as a Packet Footer (PF). The packet is buffered in a FIFO and sent to one or more D-PHY/C-PHY depending on the lane distribution scheme set by the camera sensor/user.

2.3.2 Functional Block Diagram

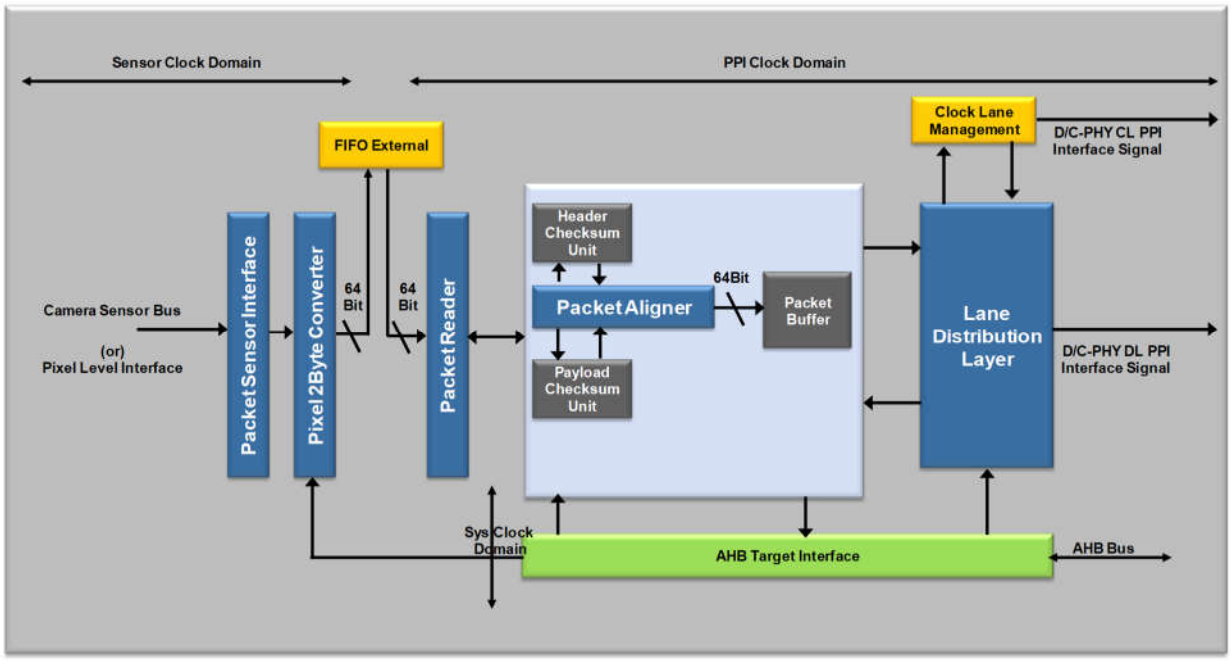


Figure 2: Combo Transmitter Functional Block Diagram

2.3.3 Configuration-64-Bit Internal Data Bus

The IP can be programmed to use with following configuration, when the internal data bus is 64-bit.

2.3.3.1 PHY Layer –DPHY

Note: The frequency of sensor clock can vary as long as the FIFO does not underflow and depends on the pixel mode/clock configuration.

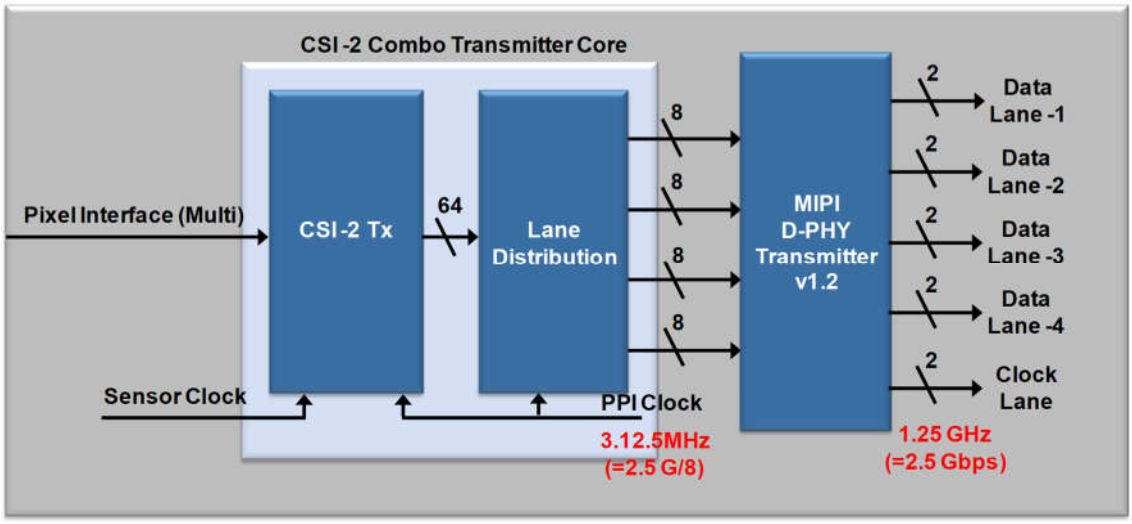


Figure 3: Combo Transmitter Usage with 4-Lane D-PHY Version 1.2

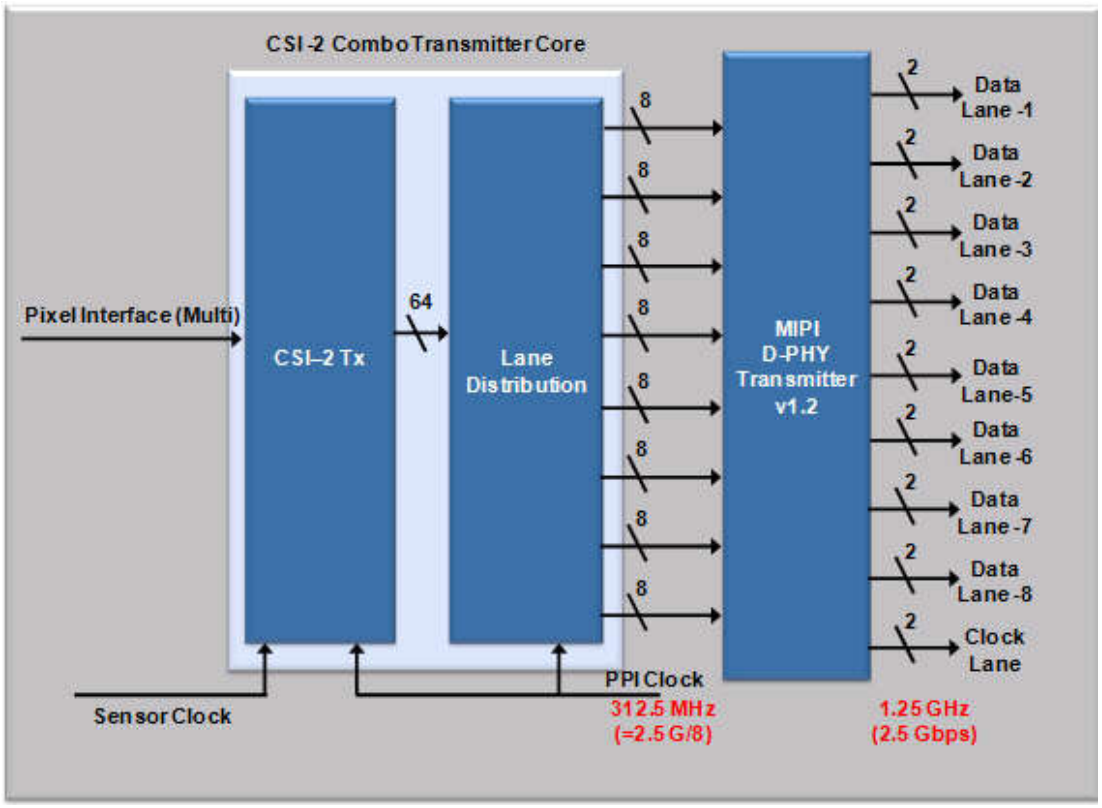


Figure 4: Combo Transmitter Usage with 8-Lane D-PHY Version 1.2

2.3.3.2 PHY Layer –CPHY

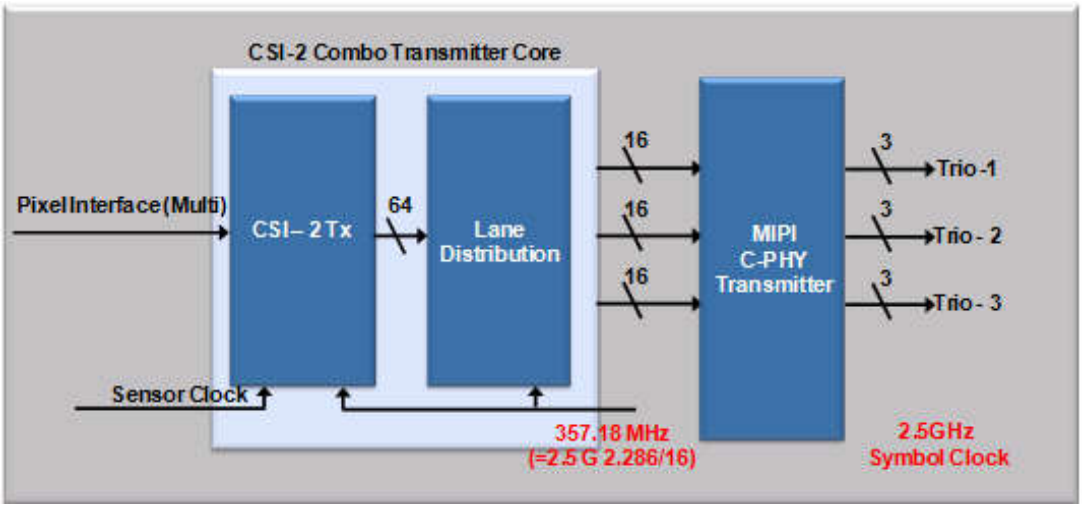


Figure 5: Combo Transmitter Usage with 3-Lane C-PHY

2.3.4 Functional Block Diagram Description

2.3.4.1 AHB Target Interface

This module connects the CSI-2 Transmitter core to external AHB processor. The user can configure the different application specific attributes through set of registers. The user can program the lanes, pixel mode and also can get status information's like FIFO status, ULPS status etc. This can be used to program both CSI-2 and PHY related registers.

2.3.4.2 Packet Sensor Interface

This module interfaces to external sensor. The module provides a handshake mechanism to accept the long pixel data packet and the synchronization packets like Frame Start (FS), Line Start (LS), Line End (LE) and Frame End (FE). This also controls the data flow from the external sensor interface to the CSI-2 Combo Transmitter Controller.

2.3.4.3 Pixel to Byte Convertor

This module converts the received pixel information to byte as per the CSI-2 specification. The respective pixel to byte convertor will get enabled based on the received data type. This module converts the received pixel information and sync packet information to 64-bit and forwards it to external memory. This module also takes care of compression of pixel information.

2.3.4.4 FIFO

This is library specific dual Port (or) Two Port RAM, which is instantiated outside the CSI-2 IP. This is used as temporary storage buffer. The size of the buffer would vary based on the application.

In cut-through mode application, which makes use of very shallow memory, this FIFO could be replaced with the register based memory. However, for store and forward architectures the size of the memory varies with the size of the resolution required. Usually for store and forward the size of the FIFO should be 2 * MAX Line size required.

2.3.4.5 Packet Reader

This module keeps track the number of packet to be processed. In cut-through mode applications, initiates the read as per the required threshold for the respective data format. Whereas in store and forward mechanism, this module waits for the complete packet to be stored in the FIFO before forwarding it to the low level protocol layer for further processing.

2.3.4.6 Low Level Protocol

This module based on the packet format received calculates the ECC/CRC for header and frames the packet header. For the received payload, calculates the CRC and appends it to the packet as packet footer.

2.3.4.7 Lane distribution Layer

This module takes care of the bytes/word distribution on to different D-PHY/C-PHY data lanes based on the user lane configuration. This will provides the PPI interface for the D-PHY/C-PHY. The clock lane layer manages the Clocks Lane PPI interface for D-PHY/C-PHY

2.4 CSI-2 Combo Transmitter Pin Diagram

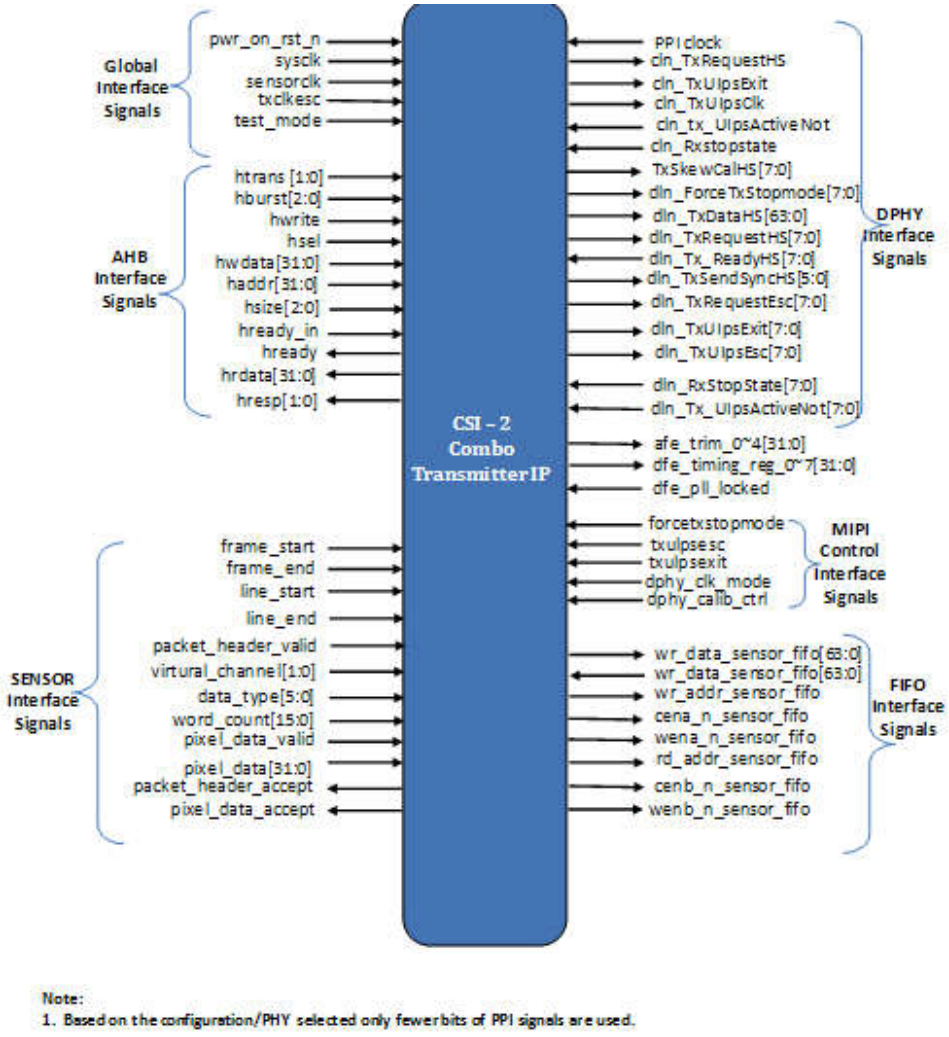


Figure 6: CSI-2 Combo Transmitter Pinout

2.5 SOC Level Integration

2.5.1 IP Deliverables

- Verilog HDL of the IP core
- User guide
- Synthesis scripts

- Lint report
- CDC report
- Verilog test suite
- Gate count estimation available upon request

2.5.2 Verification Environment

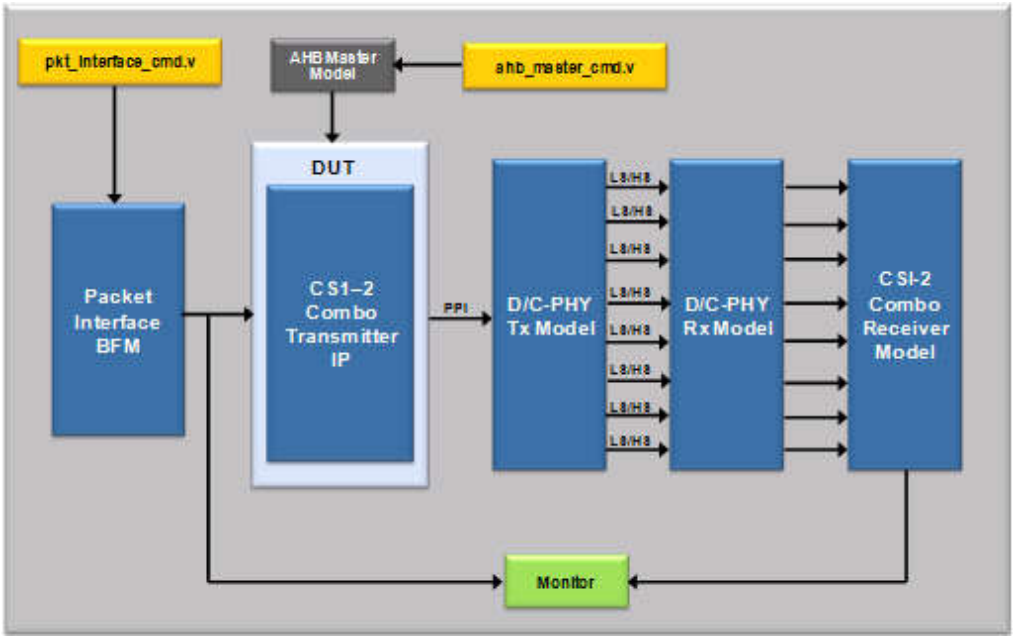


Figure 7: Verification Environment of CSI-2 Combo Transmitter IP

3 CSI-2 v1.3 Receiver IP

3.1 Overview

Arasan Chip Systems is a leading System on Chip (SoC) Intellectual Property (IP) provider of a complete suite of Mobile Industry Processor Interface (MIPI) compliant IP solutions, which consists of IP cores, verification IP, software stacks and drivers, protocol analyzers, hardware platforms(HVP's) for software development and compliance testing and optional customization services.

The Mobile Connectivity (MIPI) compliant IP cores are interface building blocks that simplify interconnect architectures in mobile platforms. This leads to smaller footprint, greater inter-operability between mobile IP, chips and devices from diverse sources and lower power and Electro Magnetic Interface (EMI).

This document describes the Arasan IP Core that functions as a MIPI Camera Serial Interface (CSI-2 Combo) Receiver, which interfaces between a peripheral device (Camera module) and a host processor (baseband, application engine). The CSI-2 Combo Receiver IP communicates over a D-PHY (or) C-PHY serial link to image processing block, part of the application engine. The Arasan CSI-2 combo IP is MIPI compliance and provides a standard, scalable, low-power, high-speed interface that supports a wide range of higher image resolutions.

3.2 Features

- Compliant with the following MIPI specifications
  - mipi_CSI-2_specification_v1-3
  - mipi_CSI-2_specification_v1-2
  - mipi_D-PHY_specification_v1-2
  - mipi_C-PHY_specification_v1-0

- CSI-2 Combo Receiver Core features:
  - Use of either D-PHY/C-PHY by user configuration
  - Different Configuration allowed for multiple use cases,
  - 4-Lane/8-Lane D-PHY / 3-Lane C-PHY
  - Lane Configurability depending on the bandwidth requirements of the application, up to 8-lanes for DPHY and up to 4-lanes for C-PHY
  - High Speed (HS) receiver rates of 182Mbps to 5714Mbps per lane with C-PHY interface
  - High Speed (HS) receiver rates of 40Mbps to 2500Mbps per lane with D-PHY interface
  - Supports for Ultra Low Power Mode (ULPS)
  - Single (or) Optional Multi-Pixel mode interface to ISP. The multi-pixel mode is used in high bandwidth requirement applications to lower the ISP clock frequency requirement.
  - Optional Pixel Level Interface to ISP with HSYNC, VSYNC, DATA and DATA VALID

- Streams the received pixels onto eight data channels(customizable) based on the channel configurability from ISP
- Separate data channel for the short generic packets
- Support for all packet level errors, Protocol Decoding Level errors
- Support for cut-though (or) store and forward mode. Cut-through mode makes use of shallow Memory for memory critical applications.
- Optional support for Compressed data formats
- Optional support for different error counting

- Pixel formats supported
  - RAW data type – RAW8, RAW10, RAW12, RAW14
  - YUV data type – YUV422-8bit, YUV422-10bit
  - RGB data type – RGB888, RGB666, RGB565, RGB555, RGB444
  - All user Defined data types / JPEG
  - Generic 8-bit long packet data types

- Host interface for register configuration and monitoring,
  - Used for programming both CSI-2 and PHY related registers. Reserved address space [0x00 – 0x0F] for the PHY related registers.
  - Optional support for the AHB/APB/Microcontroller Interface

3.3 Architecture

3.3.1 Functional Description

The Arasan CSI-2 Receiver IP is designed to provide MIPI CSI-2 v1-2/ CSI-2 v1-3 compliant high speed serial connectivity for application processors to corresponding camera modules in mobile platforms. Serial connectivity between this IP and an external camera module's CSI-2 transmitter is implemented using 1 to 8 D-PHY Lanes (or) 1 to 6 C-PHY lanes, depending on camera sensor resolutions and the application bandwidth needs. This IP connects to the D-PHY/CPHY through the PPI interface. The PPI interface of the IP is compliant to MIPI mipi_D-PHY_specification_v1-2/mipi_C-PHY_specification_v1-0. The usage of PHY's is selected by simple programming based on the use case.

Initial configuration of this IP and its associated D-PHY/C-PHY can be done through programmed IO over an AHB/APB bus. However, other bus interface can be provided upon request.

This IP performs the data lane merging of pixel data received on the PPI interface. It performs CRC and ECC checks to ensure the integrity of the packet payload and the header. Based on the PHY connected, lanes are merged accordingly and respective checks will be performed automatically. As per the application setting, IP either forwards (or) drops the erroneous packets. All forwarded packet payloads are then converted from byte to respective pixel format and output to an Image Signal Processor of the applications processor's graphics sub-system. A simple Pixel Level Interface

is used to forward the pixel information. All PHY level errors, packet level errors and decoding level errors are communicated to the HOST.

3.3.2 Functional Block Diagram

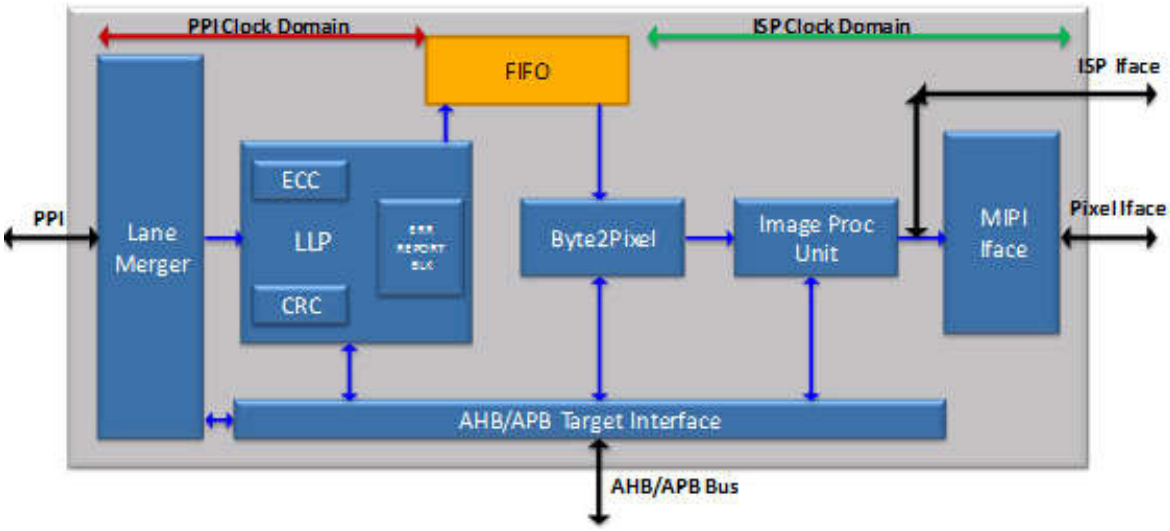


Figure 8: Functional Block Diagram

3.3.3 Configuration – 64-Bit Internal Data Bus

The IP can be programmed to use with following configuration, when the internal data bus is 64-bit.

3.3.4 PHY Layer – DPHY

The CSI-2 Combo Receiver IP can be used to configure number of lanes from 1 to 8.

Note: - The frequency of ISP clock can vary as long as the FIFO does not overflow and depends on the pixel mode/clock configuration.

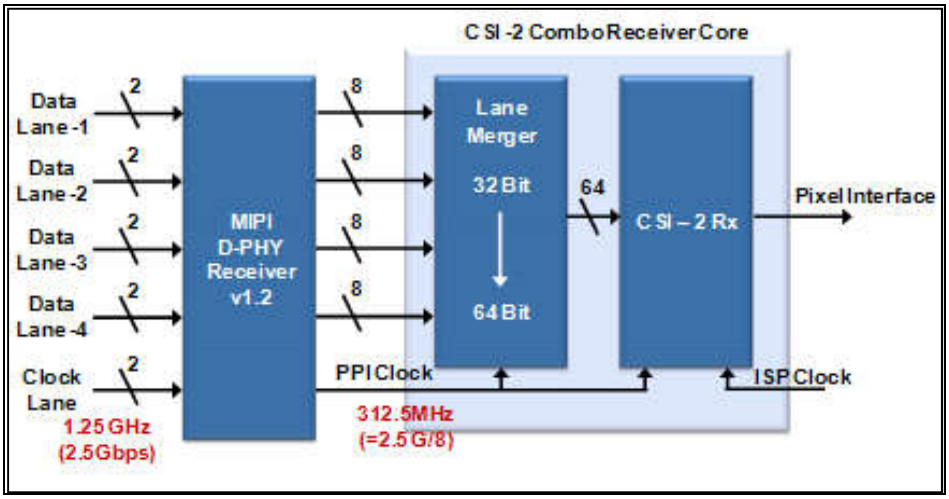


Figure 9: Combo Receiver Usage with 4 Lane D-PHY V 1.2

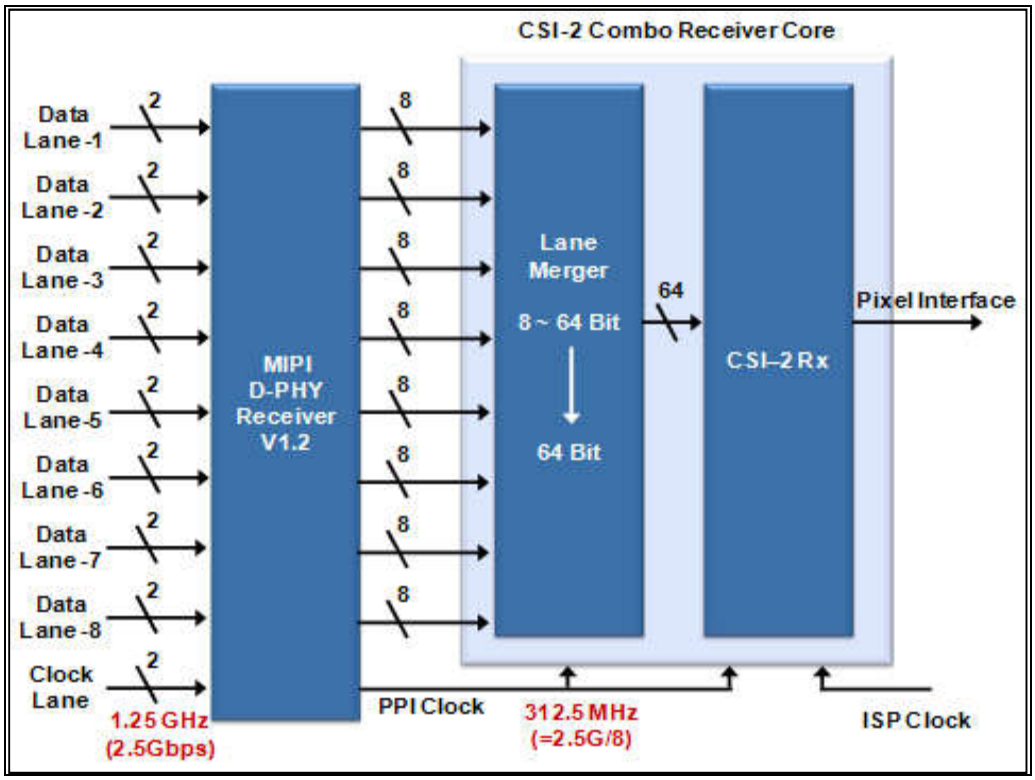


Figure 10: Combo Receiver Usage with 8 Lane D-PHY V 1.2

3.3.5 PHY Layer – C-PHY

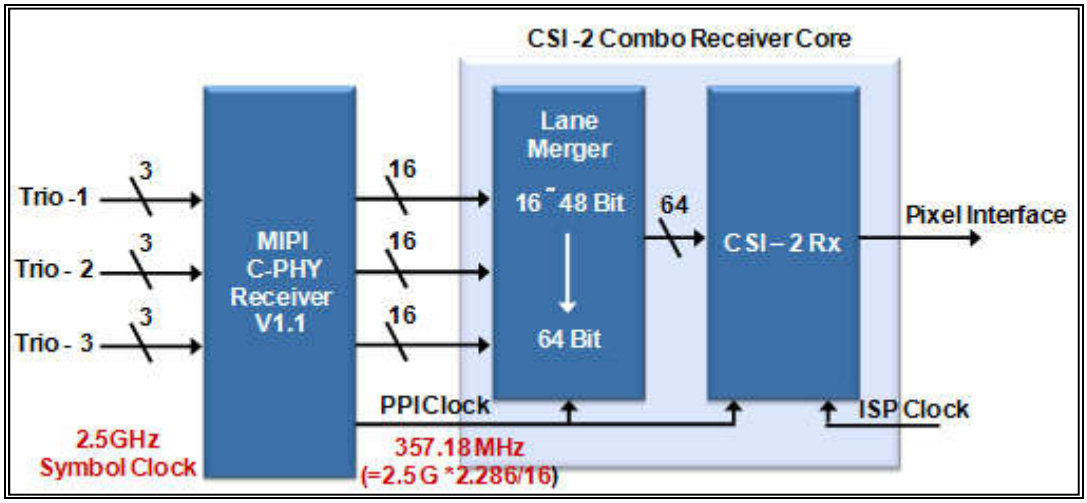


Figure 11: CSI-2 Combo Receiver Usage with 3 Lane C-PHY V 1.2

3.3.6 Functional Block Diagram Description

3.3.6.1 AHB Target Interface

This module connects the CSI-2 Receiver core to external AHB processor. The user can configure the different application specific attributes through set of registers. The user can program the lanes, pixel mode and also can get status information's like PHY level information, Packet level error information etc. This can be used to program both CSI-2 and PHY related registers.

3.3.6.2 Lane Merger

The CSI-2 Receiver is lane-scalable for increased performance. The number of data lanes may be chosen depending on the bandwidth requirement of the application. This module collects the bytes from the lanes programmed and merges them together into a recombined data stream that restores the original stream sequence. On merging the bytes, forward the stream to LLP layer for further processing. This module also handles the inter lane skew for the C-PHY application.

3.3.6.3 Low Level Protocol Unit

This module determines if the received packet is of type short (or) long. For long packets, a CRC check is performed on the payload by comparing a calculated checksum on the payload with the checksum received with packet. If connected PHY is D-PHY, an ECC check is performed on the header, single-bit errors are corrected and 2-bit errors are detected. If connected PHY is C-PHY, a CRC is performed on header received. This module also checks for all type of protocol and decoding level errors. This module takes care of interrupt generation for the critical decisions from the application. Depending on the application/use case settings, this block decides whether to forward (or) drop the erroneous packets.

3.3.6.4 FIFO

The FIFO module is used to synchronize the data flow from the LLP clock domain to ISP's clock domain. The FIFO size is configurable based on the user requirement. The FIFO size is based on the mode of operation chosen for the application. The Receiver IP adopts cut-through (or) store and forward functional modes. The cut-through requires a very shallow memory and for store and forward, memory size varies with the use case. For application, which makes use of 1 to 8 lanes DPHY and 1 to 3- lanes C-PHY, the width of the FIFO would be 64-bit. However for other configuration (6-lane C-PHY) the FIFO width required would be 96-bit. Depending on the IP configuration, the internal data bus will get change

3.3.6.5 Byte2Pixel Unit

This module unpacks the received byte stream to pixel format with respect to received data type. This module takes care of enabling respective pixel unit.

To ensure compatibility with camera modules that support data compression on RAW data types, this unit implements the two prediction and the six decompression schemes specified in the CSI-2 standard. This feature is optional and is register programmable.

3.3.6.6 Image Processor Unit

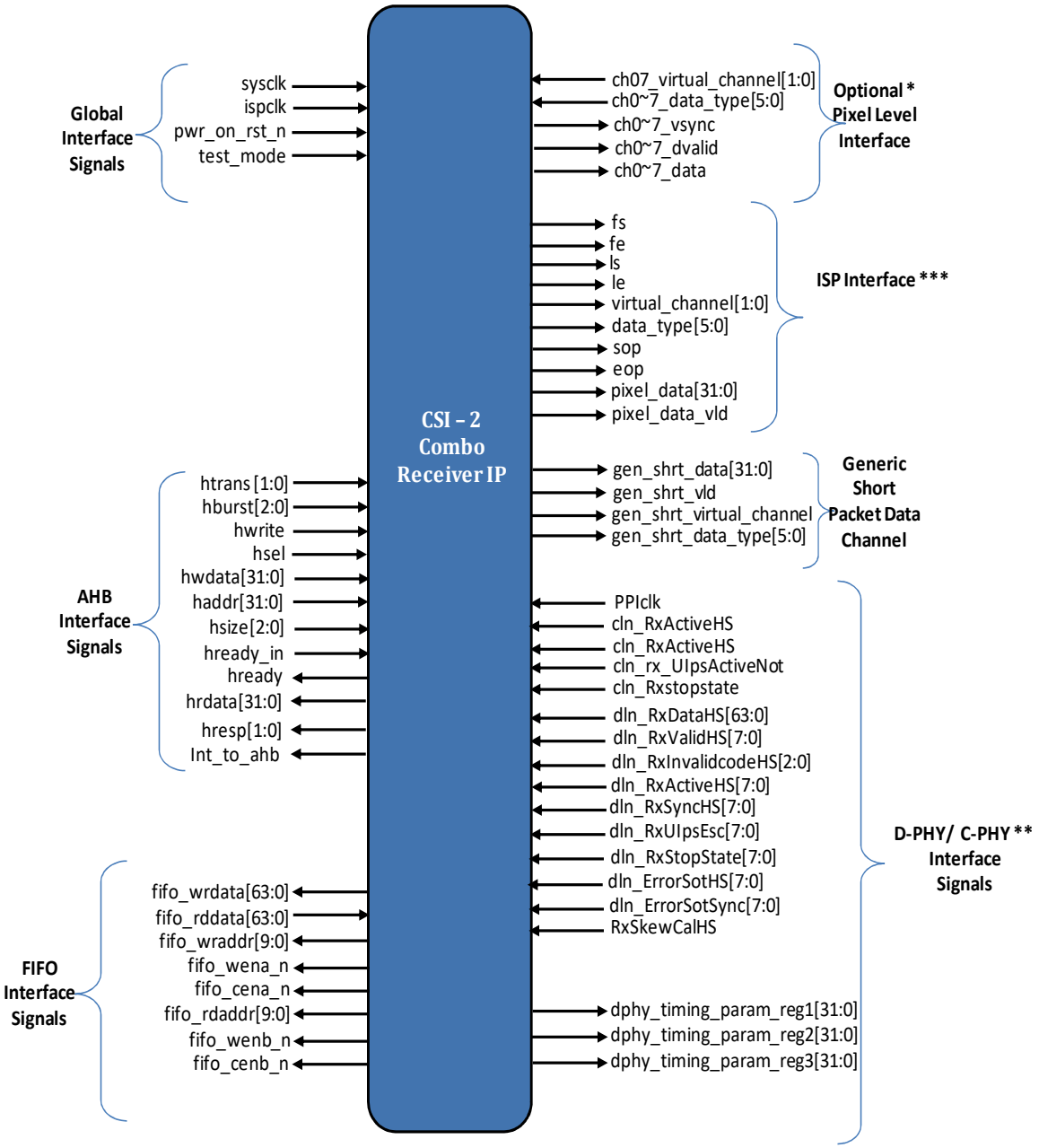
This module further processes the received pixel information and packs them into multiple pixels based on the user configuration. For high resolution application, the requirement of higher ISP clock can be reduced by adopting the multi-pixel (more than one pixel per clock) mode operation.

It also forwards control information like data type, frame number, line number, virtual channel number and packet boundary signals, namely frame start, line start, line end and frame end.

3.3.6.7 MIPI Virtual Channel Interface

This is an optional interface. This module forwards the received pixel information to configured data channel. This module interfaces to eight pixel data channels. The decision on which data channel, the received pixel to be forwarded is controlled by the external ISP. The external ISP provides 8 set of control information (each set will have virtual channel and data type). This module along with pixel data also generates HYSNC and VSYNC signals for the respective virtual channel.

3.4 CSI-2 Combo Receiver Pin Diagram



Note:
1. * If the optional Pixel Interface is enabled, the other ISP interface is disabled.
2. **Based on configuration/PHY selected only fewer bits of the PPI signals are used.
3. ***The pixel_data and valid for the ISP shown is for one pixel mode, this will be increased for the multi pixel mode.

Figure 12: CSI-2 Receiver Combo PIN Diagram

3.5 SOC Level Integration

3.5.1 IP Deliverables

- Verilog HDL of the IP Core
- User guide
- Synthesis scripts
- Link report
- CDC report
- Verilog test suite
- Gate count estimates available upon request

3.5.2 Verification Environment

- Comprehensive suite of simulation tests for ease of SoC integration
- Verification components and test files provided
- Verification environment and test suite well documented

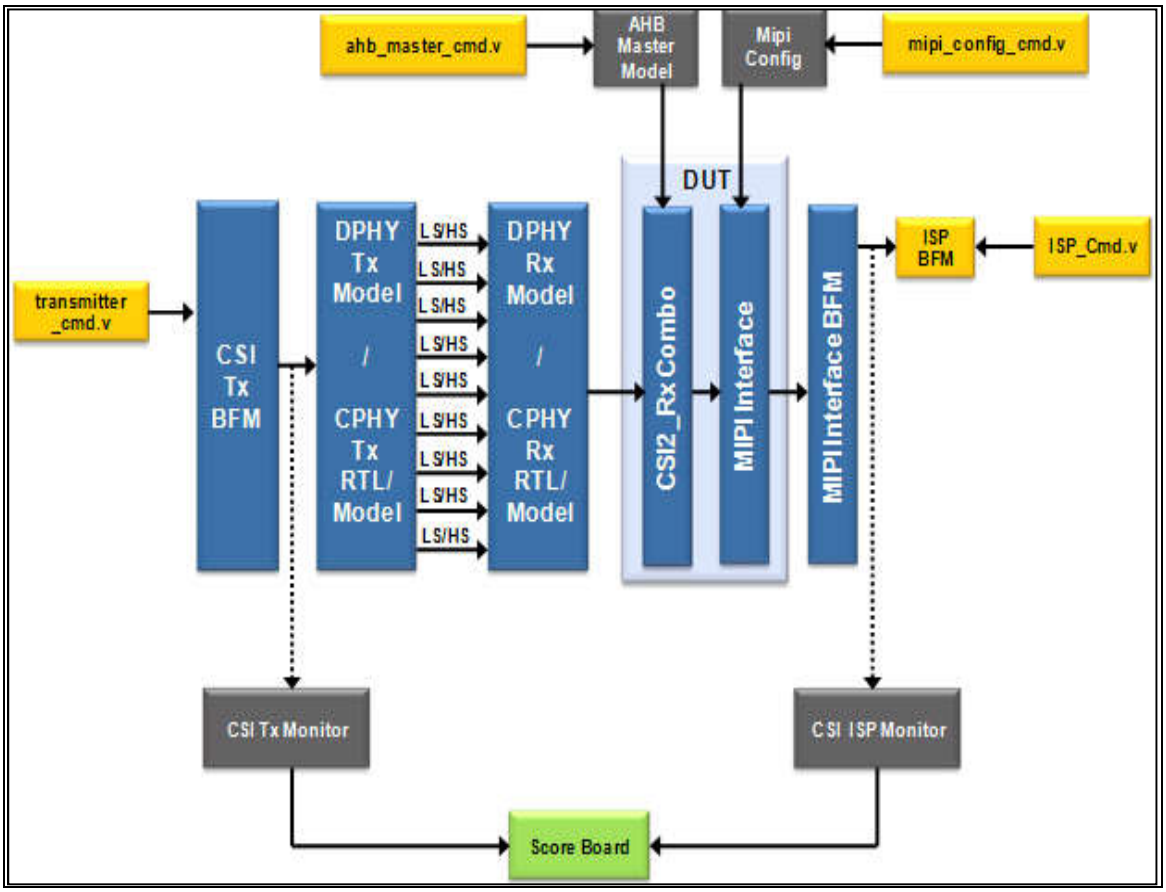


Figure 13: Verification Environment of CSI-2 Receiver IP

4 C-PHY + D-PHY Combo Physical Interface IP

4.1 Overview

The ever increasing demand for band width for the high resolution cameras resulted in to search for a simple, cost effective, rate efficient PHY which can support above 2.5Gbps. This search resulted into a new kind of PHY, which even at less channel rate provides very high data rate.

CPHY can achieve a very high data rate of 5.71Gbps per lane compared to the 2.5Gbps of DPHY1.2 or 1.5Gbps of DPHY1.1, still maintain the channel rate at 2.5Gsps which is same as DPHY1.2. CPHY achieves this by using a unique encoding mechanism in which 16 bit of input data is encoded into 7 symbols and each symbol is transmitted over a 3 Phase encoded line.

CPHY reuses the similar Low power signaling same as the DPHY. CPHY is designed such a way that it can co-exist sharing the same lines as DPHY. CPHY/DPHY combo IPs will be compatible to operate on the same channels used by DPHY, which offer a much wider area of application and flexibility. It can work with both old DPHY systems and is compatible with new CPHY.

Arasan's ComPHY is a CPHY/DPHY combo universal PHY which can be configured both as Transmitter and Receiver. Arasan's novel and innovative design techniques allowed sharing a number of modules between the CPHY and DPHY with no impact on performance resulting in optimal area and power.

4.2 C-PHY Based Interconnect Architecture

CPHY employs coding scheme in which clock can be recovered from the transmitted data. No separate clock lane is required in the interconnect and the slave will recover the clock from the data stream at the Slave side.

Each data lane is a 3 phase encoded requiring 3 separate line inter connections. Each lane interconnect provides up to 5.71 Gbps with effective data rate of 17.13 Gbps.

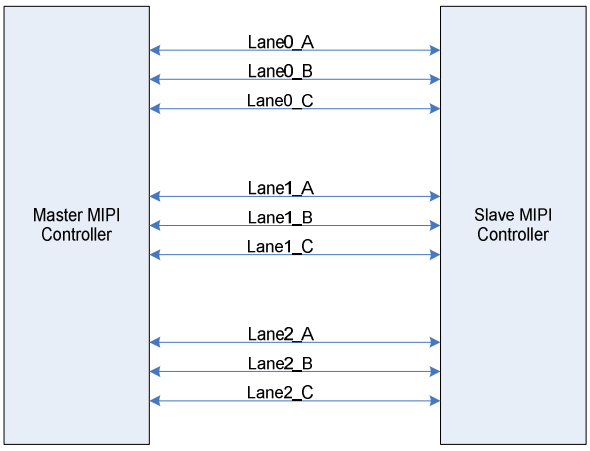


Figure 14: MIPI Link Diagram for CPHY

4.3 C-PHY Lane Architecture

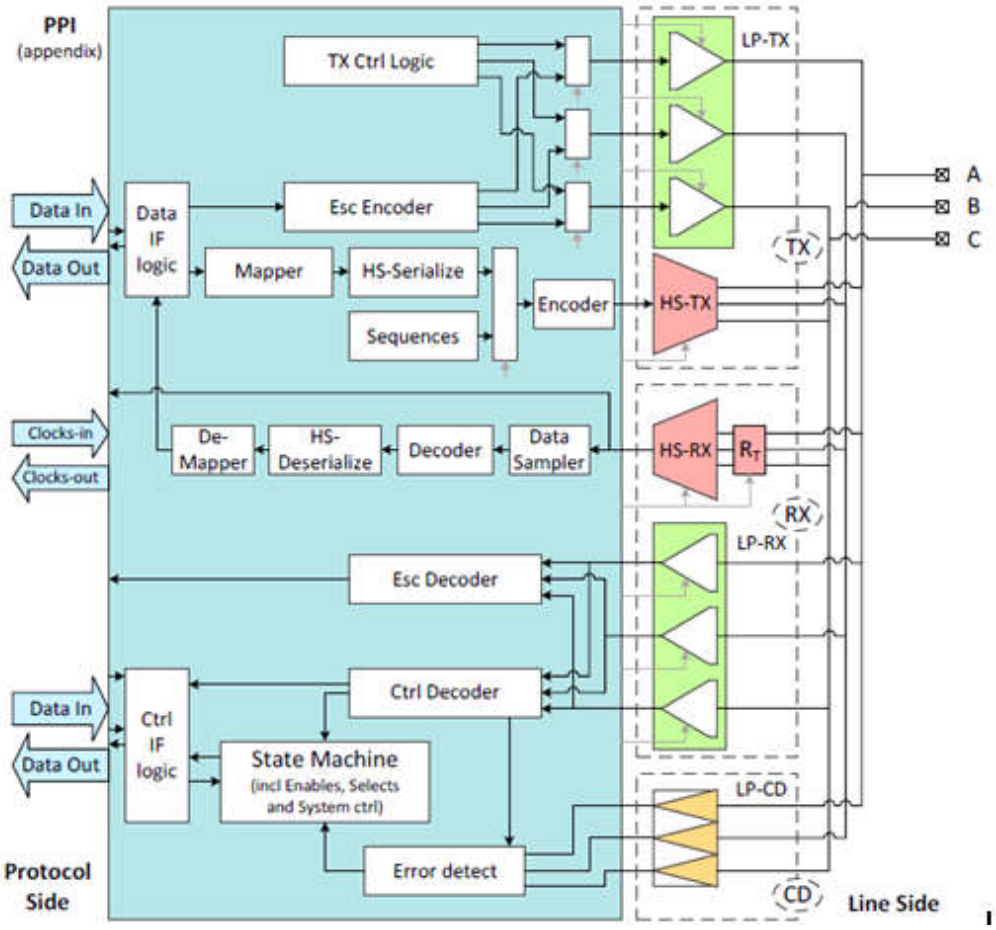


Figure 15: C-PHY Lane Architecture

Each Lane Module has a control and interface logic unit and a transceiver portion to handle 3 Phase High-Speed functions, single-ended Low-Power functions operating on each of the interconnect wires individually. The I/O functions are controlled by the Lane Control and Interface Logic block.

High-Speed signals have a low voltage swing of 250 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

High Speed data width is 16bit at the PPI side, which is converted to 7 Symbols by the mapper. Each symbol is 3 bits and it is encoded into a 3-phase signal by the encoder driver combination.

Control and Interface Logic, sends and detects start of packet signaling and end of packet signaling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

4.4 D-PHY Based Interconnect Architecture

DPHY employs a source synchronous scheme in which the High speed clock is transmitted using a separate channel along with the data lane. The clock maintains quadrature phase relationship to the data lane to ensure maximum margin between the clock and the data lane. Each data lane consists of two wires (Dp/Dn) and data is transmitted as differential signal on the both the edges of the clock.

Each lane interconnect provides up to 2.5 Gbps with effective data rate of 10 Gbps.

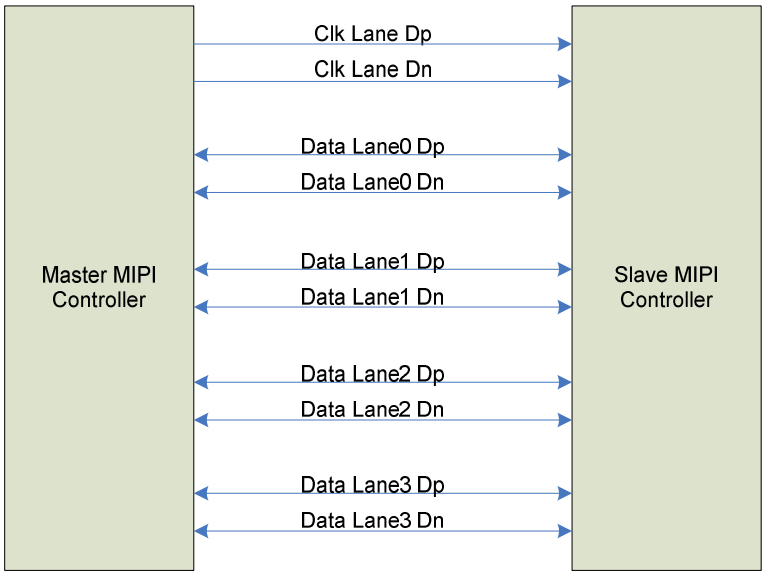


Figure 16: MIPI Link Diagram for DPHY

4.5 C-PHY – D-PHY Pad Table

Table 1: Functional description of D-PHY Pads for Clock Lane

Pin (D-PHY/ C-PHY)	Direction	Description (D-PHY)	Description (C-PHY)
dpck / lane1_A	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver	Wire A in the 3 wire lane of 1st lane
dnck / lane1_B	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver	Wire B in the 3 wire lane of 1st lane
dp2 / lane1_C	Bidirectional	Positive polarity of low voltage differential data signal for lane2	Wire C in the 3 wire lane of 1st lane
dn2 / lane2_A	Bidirectional	Negative polarity of low	Wire A in the 3 wire lane of 2nd

		voltage differential data signal for lane2	lane
dp3 / lane2_B	Bidirectional	Positive polarity of low voltage differential data signal for lane3	Wire B in the 3 wire lane of 2nd lane
dn3 / lane2_C	Bidirectional	Negative polarity of low voltage differential data signal for lane3	Wire C in the 3 wire lane of 2nd lane
dp0 / lane0_A	Bidirectional	Positive polarity of low voltage differential data signal for lane0	Wire A in the 3 wire lane of 1st lane
dn0 / lane0_B	Bidirectional	Negative polarity of low voltage differential data signal for lane0	Wire B in the 3 wire lane of 1st lane
dp1 / lane0_C	Bidirectional	Positive polarity of low voltage differential data signal for lane1	Wire C in the 3 wire lane of 1st lane
dn1	Bidirectional	Negative polarity of low voltage differential data signal for lane1	

Table 2: Power Pads

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
VDD_clk	Power	Power pad for the clock lane	Power pad for the data lane0
VSS_clk	Power	Ground pad for the clock lane	Ground pad for the data lane0
VDD_d0d1	Power	Power pad for Data lane 0 and Data lane 1	Power pad for the data lane1
VSS_d0d1	Power	Ground pad for Data lane 0 and Data lane 1	Ground pad for the data lane1
VDD_d2d3	Power	Power pad for Data lane 2 and Data lane 3	Power pad for the data lane2
VSS_d2d3	Power	Ground pad for Data lane 2 and Data lane 3	Ground pad for the data lane2
VDDD	Power	Power pad for the DFE	Power pad for the DFE
VSSD	Power	Ground pad for the DFE	Ground pad for the DFE
VDDLP12	Power	Power pad for low power block	Power pad for low power block

Table 3: Analog Function Trimming Inputs

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
trim_0[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_1[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_2[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
trim_3[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY

Table 4: Clock and Reset Inputs

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
enable	Input	Active Low system reset to the module	Active Low system reset to the module
dln_bd_ForceRx mo de	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.
dln_ForceTxStop mo de[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines	Only the first three bits are used for the CPHY. Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines

Table 5: Clock Lane High Speed PPI Interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock	-
cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal	-
TxByteClkHS / TxWordClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.	High-Speed Transmit Word Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. The same clock is shared by all lane modules. The frequency of TxWordClkHS is exactly 1/7 the high-speed symbol rate.
RxByteClkHS / RxWordClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchro-nous for receiver	High-Speed Receive Word Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock.

Table 6: Clock lane Escape PPI interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes deasserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State	-
cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line	-
cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect	-
cln_tx_UlpsActiv e Not	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-
cln_rx_UlpsActiv eN ot	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-

Table 7: Clock lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface	-

Table 8: Data lane High Speed PPI Interface Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_TxDataHS[47 :0]	Input	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock. First 32 bits are only used for DPHY	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of TxWordClkHS.
dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both	Only first three bits are used for the CPHY High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on dln_TxDataHS to be transmitted. The lane module accepts the data

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
		dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low	when both dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low
dln_TxReadyHS [3:0]	OUTPUT	High-Speed Transmit Ready for data lane. This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of transmitted byte clock	High-Speed Transmit Ready for data lane. First three bits only used for CPHY This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of TxWordClkHS
dln_TxSendSync HS[2:0]	Input	-	High Speed Command to Transmit Sync Word. This command signal has the same timing as TxDataHS[15:0] on the PPI, but when TxSendSyncHS is active on a given TxWordClkHS cycle then TxDataHS[15:0] is ignored for any Word Clock cycle where TxSendSyncHS is active.
dln_RxDataHS[47 :0]	OUTPUT	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of receiver byte clock Only first 31 bits are used for DPHY	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of RxWordClkHS

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_RxValidHS[3:0]	OUTPUT	High-Speed Receive Data Valid for data lane	High-Speed Receive Data Valid for data lane. Only first three bits are used for CPHY
dln_RxInvalidCodeHS[2:0]	Output	-	High-Speed Invalid Code Word Detection. A high-speed status signal that indicates the present word on RxDataHS[15:0] was produced by a group of seven symbols that were not a valid code word.
dln_RxActiveHS[3:0]	OUTPUT	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect. Only first three bits are used for CPHY

Table 9: Data lane Escape mode PPI Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane. dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low.	Escape mode Transmit Request for data lane. dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low. Only first three bits are used for the CPHY.
dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes deasserted.

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
		deasserted. dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.	dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State. Only first three bits are used for CPHY.
dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted.	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted. Only first three bits are used for CPHY
dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the forward direction.	This signal is used to request a low power data transmission entry in the forward direction.
dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction
dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmittedin the forward direction.	In data mode, the 8-bit data to be transmittedin the forward direction.
dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.	A valid signal which qualifies for the data lines.
dln_bd_TurnDisable	Input	To avoid the turn around request during the lock up situation	To avoid the turn around request during the lock up situation
dln_bd_Direction	Output	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_bd_TurnRequest	Input	This signal is used to request a Turn around operation for a bi-directional lane	This signal is used to request a Turn around operation for a bi-directional lane
dln_rx_RxClkEsc[3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic. Only first three bits are valid for CPHY

Table 10: Data lane Escape Mode PPI Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect. Only first three bits are used for the CPHY.
dln_rx_UlpsActiveNot[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane	ULPS signal received on the receiver in the bi-directional lane. Only first three bits are used for the CPHY.
dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction	Ready signal for the transmit data lines in reverse direction
dln_rx_RxDataEsc[7:0]	Output	The low power mode data in the Escape mode.	The low power mode datain the Escape mode.
dln_rx_RxValidEsc	Output	The ESC mode valid data	The ESC mode valid data
dln_rx_RxTrigger	Output	The Trigger mode receiver	The Trigger mode receiver signal

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
Esc[3:0]		signal	
dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane	The low power data transfer for the first lane
dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver	Error on the Escape sequence during receiver
dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode	Error in sync esc in the receiver mode

Table 11: Data lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_RxStopState [3:0]	Output	Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.	Only the first three bits are used for CPHY. Indicates Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
dln_tx_UlpsActive Not[3:0]	Output	ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.	Only the first three bits are used for CPHY. Indicates ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.
dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.	Only the first three bits are used for CPHY. Indicates Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxWordClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
dln_ErrorSotSync	Output	Start-of-Transmission	Only the first three bits are used for

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
HS[3:0]		Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.	CPHY. Indicates Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one RxWordClkHS
TxSkewCalHS	Input	Initiate the periodic deskew burst at the transmitter. A low-to-high transition on TxSkewCalHS causes the PHY to initiate a de-skew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop deskew pattern transmission and initiate an end-of-transmission sequence.	-
RxSkewCalHS	Output	High-Speed Receive Skew Calibration, which indicates the successful deskew operation to the upper layer.	-
dln_ErrContentionLP0	Output	Indicates LP0 contention on lane0.	Indicates LP0 contention on lane0.
dln_ErrContentionLP1	Output	Indicates LP1 contention on lane1.	Indicates LP1 contention on lane1.
dln_rx_ErrControl[3:0]	Output	Indicates Error control assertion in corresponding lane	Only the first three bits are used for CPHY. Indicates Error control assertion in corresponding lane

Table 12: Side Band Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
cln_pll_locked	Output	Pll locked signal from the Dphy	Pll locked signal from the Dphy

Table 13: Clock Lane PPI Control Signals

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
dln_cnt_hs_prep [7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
dln_cnt_hs_zero[7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
dln_cnt_hs_trail[7:0]	Input	The period for which HS Trail time should be accommodated for data lane in Byte clock period	The period for which HS trail time should be accommodated for data lane in Word clock period
dln_cnt_hs_exit[7:0]	Input	The period for which HS Exit time should be accommodated for data lane in Byte clock period	The period for which HS exit time should be accommodated for data lane in Word clock period
dln_rx_cnt[7:0]	Input	Counter that controls the assertion of enable on the DPHY for data lanein Byte clock period	Counter that controls the assertion of enable on the DPHY for data lane in Word clock period
dln_sync_cnt[7:0]	Input	A timeout value used for sync error detector logic for data lane in Byte clock period	A timeout value used for sync error detector logic for data lane in Word clock period
dln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period	The time period in which LP states are driven in Byte clock period
cln_cnt_hs_trail[7:0]	Input	The period for which HS trail time should be accommodated for clock lane in Byte clock period	-
cln_cnt_hs_exit[	Input	The period for which HS exit	-

Pins (DPHY/ CPHY)	Direction	Description (DPHY)	Description (CPHY)
7:0]		time should be accommodated for clock lane in Byte clock period	
cln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period for clock lane	-
cln_cnt_prep[7:0]	Input	The period for which HS prepare time should be accommodated for clock lane in Byte clock period	-
cln_cnt_zero[7:0]	Input	The period for which HS zero time should be accommodated for clock lane in Byte clock period	-
cln_cnt_pll[15:0]	Input	The count value which is used for the PLL lock time	The count value which is used for the PLL lock time

4.6 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and integration guides
- LEF
- Scan-inserted netlist for DFT
- Verification environment with behavioral models
- IBIS models

5 D-PHY v1.2 Physical Interface IP

5.1 Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI®) Alliance was created to define and promote open standards for interfaces to mobile application processors. D-PHY is the physical layer specified for several of the key protocols within the MIPI® family of specifications.

The Arasan D-PHY IP core is fully compliant to the D-PHY specification version 1.2. It supports the MIPI® Camera Serial Interface (CSI-2) and Display Serial Interface (DSI) protocols. It is a universal PHY that can be configured as a transmitter, receiver or transceiver. The D-PHY consists of an analog front end to generate and receive the electrical level signals, and a digital back end to control the I/O functions.

The Arasan D-PHY provides a point to point connection between master and slave or host and device that comply with a relevant MIPI® standard. A typical configuration consists of a clock lane and 1-4 data lanes. The master/host is primarily the source of data and the slave/device is usually the sink of data. The D-PHY lanes can be configured for unidirectional or bidirectional lane operation, originating at the master and terminating at the slave. It can be configured to operate as a master or as a slave. The D-PHY link supports a high speed (HS) mode for fast data traffic and a low power (LP) mode for control transactions. In HS mode, the low swing differential signal is able to support data transfers from 80 Mbps to 1500 Mbps per lane without deskew calibration and up to 2500 Mbps with deskew calibration. In LP mode all wires operate as a single ended line capable of supporting 10 Mbps asynchronous data communications.

The Arasan D-PHY IP core implements the PPI interface recommended by the MIPI® working groups to easily interface to the required protocols.

D-PHY v1.2 is compatible with CSI-2 v1.3 and earlier versions back to CSI-2 v1.1. D-PHY v1.2 is compatible with DSI v1.3 and DSI-2 v1.0 and prior versions back to DSI v1.1

5.2 Features

- Compliant to MIPI Alliance Standard for D-PHY specification Version 1.2. Supports:
- Synchronous transfer at high speed mode with a bit rate of 80-2500 Mb/s
- Asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low Power [LP] data
- One byte buffer housed inside the core for both data-out and data-in paths.
- One clock lane and up to four data lanes
- Error detection mechanism for sequence errors and contentions
- Transfer of data in high speed mode
- Ultra low power mode, high speed mode and escape mode.

- Contention detection and turnarounds
- Clock divider unit to generate clock for parallel data reception and transmission from and to the PPI unit.
- Activation and disconnection of high speed terminators for reception and transmission.
- Standard PHY transceiver compliant to MIPI Specification
- Standard PPI interface compliant to MIPI Specification.
- Clock lane unidirectional communication
- On-chip clock generation configurable for either transmitter or a receiver
- Testability for Tx, Rx and PLL
- Configurability of PHY as a master or slave
- Core structured to increase the number of data lanes
- High speed mode in Forward communication

5.3 Architecture

5.3.1 D-PHY Based Interconnect Architecture

Physical connectivity between a master and slave component requires a clock lane and, depending on bandwidth needs, one to four data lanes. To support this, a D-PHY has a Clock Lane Module, and one to four Data Lane Modules. Each of these D-PHY Lane Modules communicates via a differential signal pair to a complementary part on the other side of the Lane Interconnect.

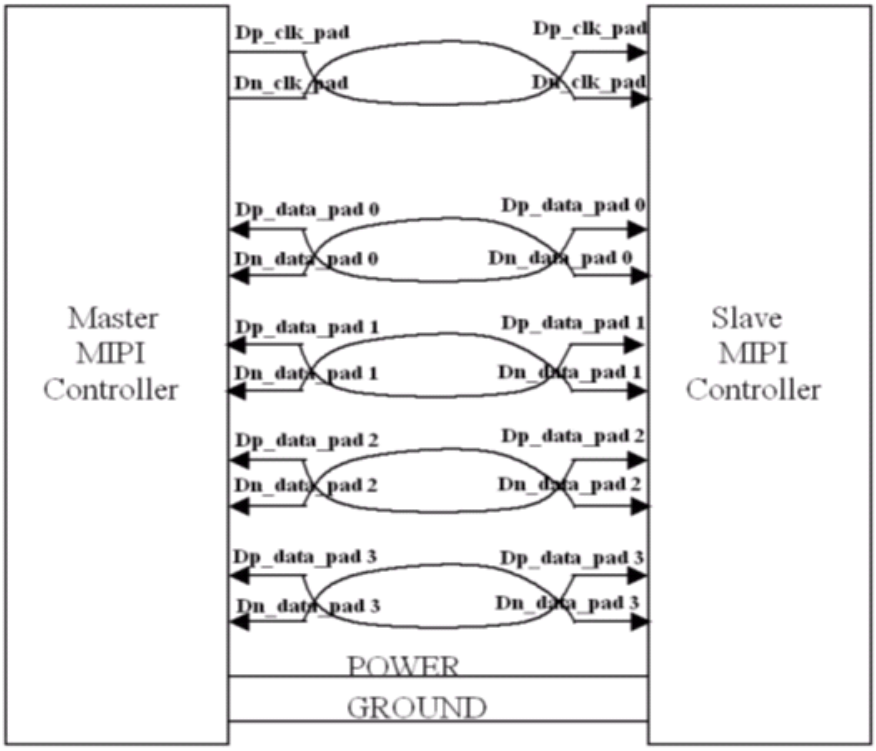


Figure 17: MIPI Link Diagram for Four Data Lanes

5.3.2 D-PHY Lane Architecture

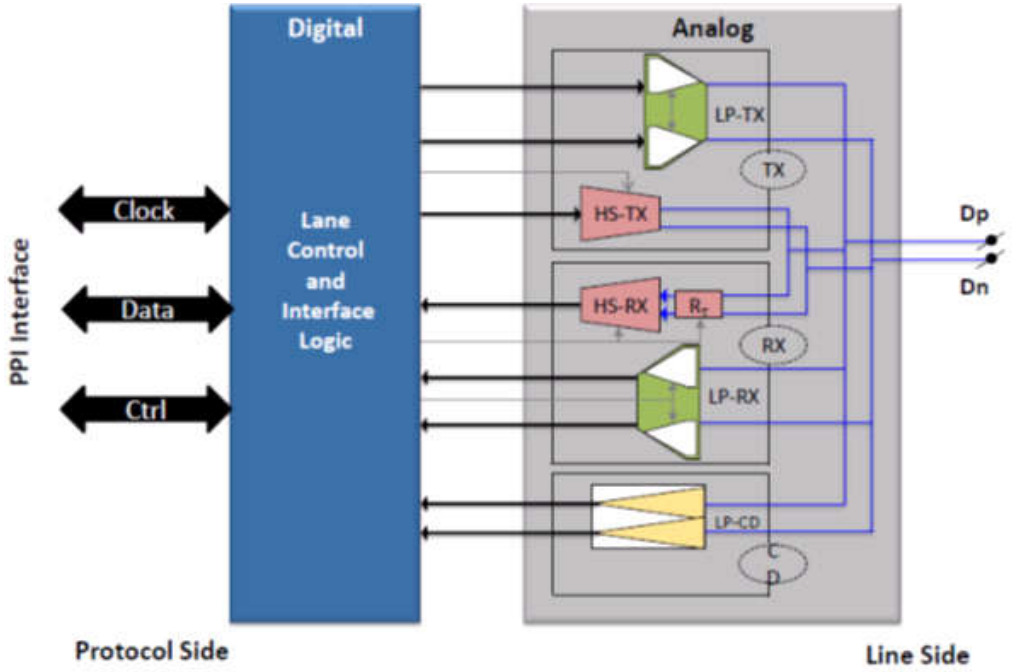


Figure 18: D-PHY Lane Architecture

5.3.2.1 Lane

Each Lane Module has a control and interface logic unit and a transceiver portion to handle differential High-Speed functions utilizing both interconnect wires simultaneously, single-ended Low-Power functions operating on each of the interconnect wires individually and a low power contention detector. The I/O functions are controlled by a Lane Control and Interface Logic block.

5.3.2.2 Signaling

High-Speed signals have a low voltage swing of 200 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

5.3.2.3 Link

Each link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the main data sink. This main direction of communication is denoted as the Forward direction. Communication in the opposite direction is called Reverse traffic. Only bi-directional Data Lanes support both forward and reverse communications.

5.3.2.4 Lane Control and Interface Logic

It sends and detects start of packet signalling and end of packet signalling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

5.4 Arasan D-PHY Architecture

The transceiver pins of the Arasan D-PHY are compliant to MIPI's transceivers. The lane control and interface logic unit operates with the clock provided by PPI unit during high speed as well as in low power modes of operation in master mode whereas, a separate low power clock is used in slave mode for low power operations and the received high speed clock is used for high speed data transfers.

In Arasan D-PHY digital IP, both Master and slave modes have state machines to generate sequences for switching to high speed, control mode and ultra low power modes. They have deserializer/serializer unit to convert parallel to serial data and vice-versa.

Slave device has sequence observer state machines to know the modes of operation of the lanes. They have sequence error detectors also.

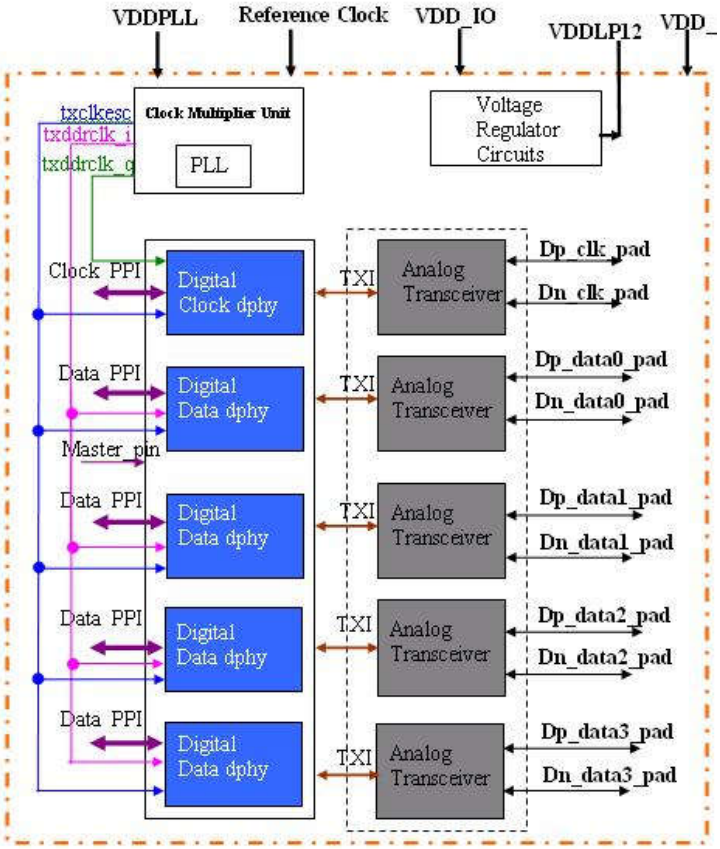


Figure 19: Analog and Digital D-PHY Block Diagram

5.5 D-PHY Pad Table

5.5.1 Functional Description of D-PHY Pads for Clock Lane

Table 14: Functional Description of D-PHY Pads for Clock Lanes

Pin	Direction	Description
dpck	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver
dnck	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver

5.5.2 Functional Description of D-PHY Pads for First Data Lane

Table 15: Functional Description of D-PHY Pads for First Data Lane

Pin	Direction	Description
dp0	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn0	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.3 Functional Description of D-PHY Pads for Second Data Lane

Table 16: Functional Description of D-PHY Pads for Second Data Lane

Pin	Direction	Description
dp1	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn1	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.4 Functional Description of D-PHY Pads for Third Data Lane

Table 17: Functional Description of D-PHY Pads for Third Data Lane

Pin	Direction	Description
dp2	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn2	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.5 Functional Description of D-PHY Pads for Fourth Data Lane

Table 18: Functional Description of D-PHY Pads for Fourth Data Lane

Pin	Direction	Description
dp3	Bidirectional	Positive polarity of low voltage differential data signal for transmitter and receiver
dn3	Bidirectional	Negative polarity of low voltage differential data signal for transmitter and receiver

5.5.6 Power Pads

Table 19: Power Pads

Pin	Type	Direction	Description
VDD_clk	Power	InOut	Power pad for Clock lane
VSS_clk	Power	InOut	Ground pad for Clock lane
VDD_d0d1	Power	InOut	Power pad for Data lane 0 and Data lane1
VSS_d0d1	Power	InOut	Ground pad for Data lane 0 and Data lane1
VDD_d2d3	Power	InOut	Power pad for Data lane 2 and Data lane 3
VSS_d2d3	Power	InOut	Ground pad for Data lane 2 and Data lane 3
VDDD	Power	InOut	Power pad for DFE
VSSD	Power	InOut	Ground pad for DFE
VDDLP12	Power	InOut	Power pad for Low power blocks

5.5.7 Functional Description of Trim Bits

Table 20: Ports for Trim_Bits

Pin	Direction	Description
trim_0[31:0]	Input	Trim bits for DPHY
trim_1[31:0]	Input	Trim bits for DPHY
trim_2[31:0]	Input	Trim bits for DPHY
trim_3[31:0]	Input	Trim bits for DPHY

5.5.8 Functional Description of Clock and Reset Unit Input

Table 21: Functional Description of Clock and Reset unit Input signals for clock and data PPI

Pin	Direction	Description
TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
enable [Reset]	Input	Active Low system reset to the module.

5.5.9 Functional Description of Data PPI Signals Common to all Data Lanes

Table 22: Functional Description of data PPI signals that are common to all Data Lanes

Pin	Direction	Description
dln_bd_ForceRxmode	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.
dln_ForceTxStopmode[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines.

5.5.10 Functional Description of Clock PPI's Escape Mode Signals

Table 23: Functional Description of Clock PPI's High Speed Interface Signals

Pin	Direction	Description
cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock.
cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal
TxByteClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.

RxByteClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchronous for receiver.
RxDDRClkHS_0	Output	High speed DDR clock used by the receiver.
cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes deasserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State
cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line.
cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect
cln_tx_UlpsActive Not	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state.
cln_rx_UlpsActiveN ot	Output	ULP State (not) Active for clock lane. This active low signal is asserted to indicate that the Lane is in ULP state

5.5.11 Functional Description of Clock PPI's Control Signals

Table 24: Functional Description of Clock PPI's Control Signals

Pin	Direction	Description
cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface

5.5.12 Functional Description of Clock PPI's High Speed Interface Signals

Table 25: Functional Description of Data PPI's High Speed Interface signals

Pin	Direction	Description
dln_TxDataHS[31:0]	Input	High-Speed Transmit Data for data lane. High-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock.
dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on txrequesths causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on txrequesths causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both txrequesths and txreadyhs are active on the same rising txbyteclkhs clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, txdatahs remains high until the data has been accepted, as indicated by txreadyhs. txdatahs is only asserted while txrequestesc_0 is low
dln_TxReadyHS [3:0]	Output	High-Speed Transmit Ready for data lane. This active high signal indicates that txdatahs_0 is accepted by the lane module to be serially transmitted. txreadyhs_0 is valid on rising edges of transmitted byte clock.
dln_RxDataHS[31:0]	Output	High-Speed Receive Data for data lane. The signal connected to rxdatahs_0 was received first. Data is transferred on rising edges of receiver byte clock.
dln_RxValidHS[3:0]	Output	High-Speed Receive Data Valid for data lane.
dln_RxActiveHS [3:0]	Output	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.
dln_RxSyncHS[3:0]	Output	Receiver Synchronization Observed for data lane. This active high signal indicates that the Lane module has seen an appropriate synchronization event. In a typical high-speed transmission, rxsynchs_0 is high for one cycle of received byte clock at the beginning of a high-speed transmission when rxactivehs_0 is first asserted, and again for one cycle of received byte clock at the end of a high-speed transmission, just before rxvalidhs_0 returns low.

5.5.13 Functional Description of Data PPI's Escape Mode Signals

Table 26: Functional Description of Data PPI's Escape mode Signals

Pin	Direction	Description
dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane . txrequestesc_0 is only asserted by the protocol while txrequesths_0 is low.
dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane 0. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes deasserted. txulpsexit_0 is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State.
dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane 0. This active high signal is asserted with txrequestesc to cause the lane module to enter the ultra-low power mode. The lane module remains in this mode until txrequestesc_0 is deasserted. txlpdtesc_0 and all bits of txtriggeresc are low when txulpsesc_0 is asserted.
dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the reverse direction.
dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the reverse direction.
dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmitted in the reverse direction.
dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.
dln_bd_TurnDisable	Input	To avoid the turn-around request during the lock up situation.
dln_bd_Direction	OutPut	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input).
dln_bd_TurnRequest	Input	This signal is used to request a turn-around operation for a bidirectional lane.
dln_rx_RxClkEsc [3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic.

Pin	Direction	Description
dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra-low power mode. The lane module remains in this mode with rxulpsesc asserted until a Stop state is detected on the lane interconnect.
dln_rx_UlpsActiveNot[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane
dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction.
dln_rx_RxDataEsc[7:0]	Output	The low power mode data in the Escape mode.
dln_rx_RxValidEsc	Output	The ESC mode valid data.
dln_rx_RxTriggerEsc[3:0]	Output	The Trigger mode receiver signal.
dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane
dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver
dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode.

5.5.14 Functional Description of Data PPI's Control Signals

Table 27: Functional Description of Data PPI's Control Signals

Pin	Direction	Description
dln_RxStopState[3:0]	Output	Lane is in Stop state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
dln_tx_UlpsActiveNot[3:0]	Output	ULP State (not) Active for data lane. This active low signal is asserted to indicate that the Lane is in ULP state.
dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
dln_ErrorSotSyncHS[3:0]	Output	Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted

Pin	Direction	Description
		in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.
dln_ErrContention LP0	Output	The contention error signal on LP0 line.
dln_ErrContention LP1	Output	The contention error signal on LP1 line.
dln_rx_ErrControl [3:0]	Output	Error control in lane 0 during receiver

5.5.15 Functional Description of Side Band Signals

Table 28: Functional Description of Side Band Signals

Pin	Direction	Description
dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
dln_dpdnswap[3:0]	Input	Enable dp dn swap on data lanes 0 to 3 in HS Tx mode.
cln_pll_locked	Output	Pll locked signal from the Dphy

5.5.16 Functional Description of DFT Signals

Table 29: Functional Description of DFT Signals

Pin	Direction	Description
SCAN_EN	Input	Scan mode Enable.
SCAN_CLK	Input	Scan clock
SA_SCAN	Input	Stuck-At scan mode.
SCAN_IN	Input	Scan input for At-speed scan.
SCAN_OUT	Output	Scan output for At-speed scan.
DFT_sdi_1 to 6	Input	Scan input for At-speed scan.
DFT_sdo_1 to 6	Output	Scan output for At-speed scan.

5.5.17 D-PHY UI Parameter Count Signals

Table 30: D-PHY UI Parameter Count Signals

Pin	Type	Direction	Description
dln_cnt_hs_prep[7:0]	Register	Input	The period for which HS prepare time should be accommodated for data lane[40ns]
dln_cnt_hs_zero[7:0]	Register	Input	count [260ns] for Tclock count.
dln_cnt_hs_trail[7:0]	Register	Input	The period for which HS trailing should be driven for data lane[60ns].
dln_cnt_hs_exit[7:0]	Register	Input	The period for which HS exit state should be maintained for data lane[110ns].
dln_rx_cnt[7:0]	Register	Input	Counter that controls the assertion of enable on the DPHY for data lane
dln_sync_cnt[7:0]	Register	Input	A timeout value used for sync error detector logic for data lane.
dln_cnt_lpx[7:0]	Register	Input	Wait time in byte data for the LPX for data lane.
cln_cnt_hs_trail[7:0]	Register	Input	Wait time in byte clock for the trailing bits for clock lane[60ns].
cln_cnt_hs_exit[7:0]	Register	Input	wait time in byte clock for the exit state for clock lane[110ns]
cln_cnt_lpx[7:0]	Register	Input	wait time in byte clock for the LPX for clock lane.
cln_cnt_prep[7:0]	Register	Input	wait time in byte clock for the prepare time for clock lane[40ns]
cln_cnt_zero[7:0]	Register	Input	wait time in byte clock for the zero state for clock lane[260ns].
cln_cnt_pll[15:0]	Register	Input	The count value which is used for the PLL lock time.
dln_cnt_lpx[7:0]	Register	Input	The period for which the LP state should be driven.

5.5.18 A-BIST Related Signals

Table 31: A-BIST Pins

Pin	Direction	Description
dln_loop_back	Input	Enable A-BIST (loopback BIST)
bist_seed[7:0]	Input	BIST PRBS intiation seed
bist_force_error	Input	Signal is used to introduce errors in the BIST run.

Pin	Direction	Description
bist_en_esc_lp, bist_en_esc_hs	Input	Bist mode selection pins 00-> Reserved 01-> HS Mode 10-> LP Mode 11-> RxClkEsc Generation
bist_err_rx_hs	Output	Error in HS reception
bist_err_rx_hs_sync	Output	Error in RX HS sync
bist_err_rx_esc	Output	Error in LP reception
bist_err_rx_esc_ sync	Output	Error in LP rx sync
bist_done	Output	End of BIST comparison

5.6 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User-guide and integration guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models

6 Services & Support

6.1 Global Support

Arasan Chip Systems provide global support to its IP customers. The technical support is not geographically bound to any specific site or location, and therefore our customers can easily get support for design teams that are distributed in several locations at no extra cost.

6.2 Arasan Support Team

Our technical support is provided by the engineers who have designed the IP. That is a huge benefit for our customers, who can communicate directly with the engineers who have the deepest knowledge and domain expertise of the IP, and the standard to which it complies.

6.3 Professional Services & Customization

At Arasan Chip Systems we understand that no two Application Processors are the same. We realize that often the standard itself needs some tweaks and optimizations to fit your design better. Sometimes, the interface between the IP blocks and your design need some customization. Therefore, we provide professional services and customization to our IP customers. We do not sell our IP blocks as “black box” that cannot be touched. Please contact us for more details on our customization services.

6.4 The Arasan Porting Engine

Analog IP blocks, such as eMMC 5.1 HS400 PHY, are designed for a specific Fab and process technology. Arasan’s analog design team, utilizing its deep domain expertise and vast experience, is capable of porting the PHYs into any specific process technology required by the customer. That is “The Arasan Porting Engine”.

6.5 Pricing & Licensing

Arasan charges a one-time licensing fee, with no additional royalties. The licensing fee gives the right to use our IP for 1 project. Licensing fee for additional projects, using the same IP, is discounted. We also offer unlimited-use license. For any additional information regarding pricing and licensing – please contact our sales at: sales@arasan.com.