DATASHEET

Universal Asynchronous Receiver/Transmitter (UART) Controller

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CONTENTS

TABLES

FIGURES

1 INTRODUCTION

The Arasan 16550D High Speed UART IP core is a16550-compliant Universal Asynchronous Receiver/Transmitter (UART) with FIFO or expanded FIFO. UART complies to the standard 16550D with FIFOs. The UART performs serial to parallel conversion of the data received from the external device and parallel to serial conversion of data received from the AHB bus Interface. It supports both character and FIFO modes. The complete status of the UART can be read from its registers

1.1 Overview

The UART performs serial to parallel conversion of data received from the serial interface, and parallel to serial conversion of data received from the CPU interface. Both character and FIFO modes are supported. Operation of the UART can be programmed by a host processor through the host interface. Writing to the Control register determines the operational mode of the UART. The transmitter and receiver at the serial interface perform parallel to serial and serial to parallel conversion of data. Baud rate clock and receiver reference clock are generated by the Baud Rate Generator.

Writing to the Divisor Latch Registers (DLL and DLM) controls the clock rate. The interrupt controller signals the host processor in the event of error conditions such as transmission errors or modem status changes.

Complete status of the UART can be accessed by the host processor at any time. The Status registers provide information such as the modem status, line condition, line break, overrun, parity error, and other conditions.

The 16550D High Speed UART IP core implements a UART on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications. The Arasan 16550D High Speed UART IP core has been widely used in different applications by major chip vendors.

1.2 Features

- Complies with UART 16550D specification
- Complies with SD_PHS Specification Ver1.0
- Supports character mode, FIFO mode, and extended FIFO mode
- Maximum 255 bytes FIFO size
- Programmable baud rate generator
- Maximum baud rate up to 1Mb/s
- 5-, 6-, 7-, or 8-bit per character
- 1, 1.5, or 2 stop bits.
- Even, odd, or stick parity
- Interrupt controller
- Complete status reporting

2 ARCHITECTURE

The architecture diagram of the UART IP is shown below.

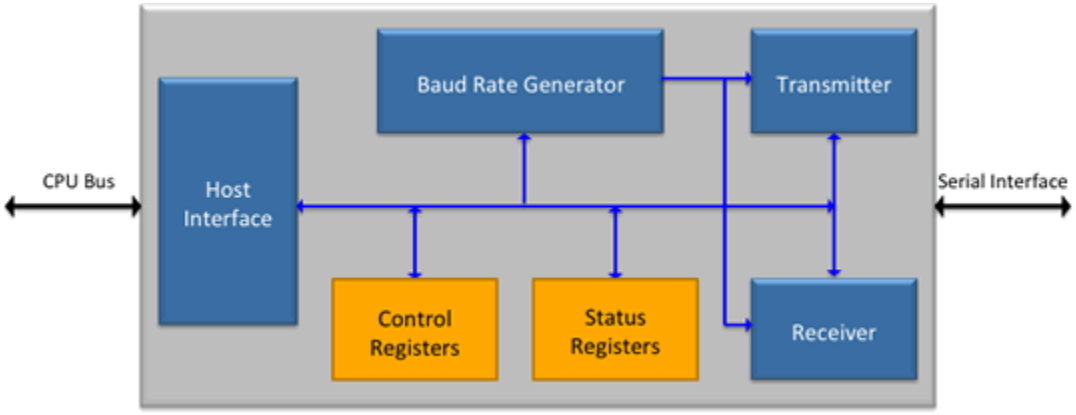


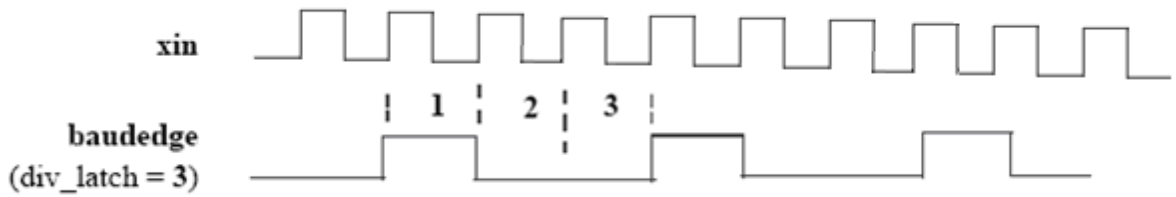
Figure 1: UART IP Block Diagram

2.1 Host Interface

This block interfaces between the AHB bus master and UART. This merely acts as a AHB bus bridge. This works as a target module which functions according to the commands of AHB master model. It works in hclk. There are synchronizers for the control signals from the hclk to the UART clock.

2.2 Baud Rate Generator

The UART controller contains programmable baud generator that is capable of taking any clock input from DC to 24Mhz and dividing it by any divisor from 2 to 216-1. The output frequency of baud generator is 16 x the baud. This baud edge is used by transmit and receive blocks. Divisor latch value can be calculated by using the following formula
Divisor = frequency input / (baud rate x 16)



2.3 Transmitter

This block converts the parallel data into serial data, adds the overhead bits and transmits through SOUT. The FIFO size for transmit is 256 bytes. An empty interrupt is generated when there is space for 16 bytes of data when extended FIFO enable bit is disabled. An empty interrupt is generated when there is space for 256 bytes of data when extended FIFO bit is enabled.

The three bit is set only when the FIFO is fully empty, that is when the last data is shifted to the transmit shift register (TSR). The TEMT bit is sent only when the stop bit of the last data has been fully transmitted. Number of stop bits, parity bit, and number of data bits can be controlled through the line control register. Data set ready and clear to send handshaking is checked in transmit block. Both FIFO mode and character mode are taken care.

2.4 Receiver

This block receives the serial data and converts it into parallel data. FIFO size is 256 bytes. These trigger levels are programmed by the software through the FIFO control register. Framing error and brake interrupt error recovery is taken care in receiver. Parity checking and overrun error checking is handled. Each serial bit is sampled at the centre point. Time out interrupt is generated for both read and write timeouts. Both FIFO mode and character mode is taken care.

Trigger level	Extended FIFO enable bit is‘1’	FIFO enable bit is ‘1’
2’b00	32	1
2’b01	64	4
2’b10	128	8
2’b11	192	14

2.5 Registers

This block decodes the address from the AHB bus to control all the UART Registers. All UART register’s read and write takes place in this module. This also takes care of all read only, write only and read/write registers.

3 PIN DIAGRAM

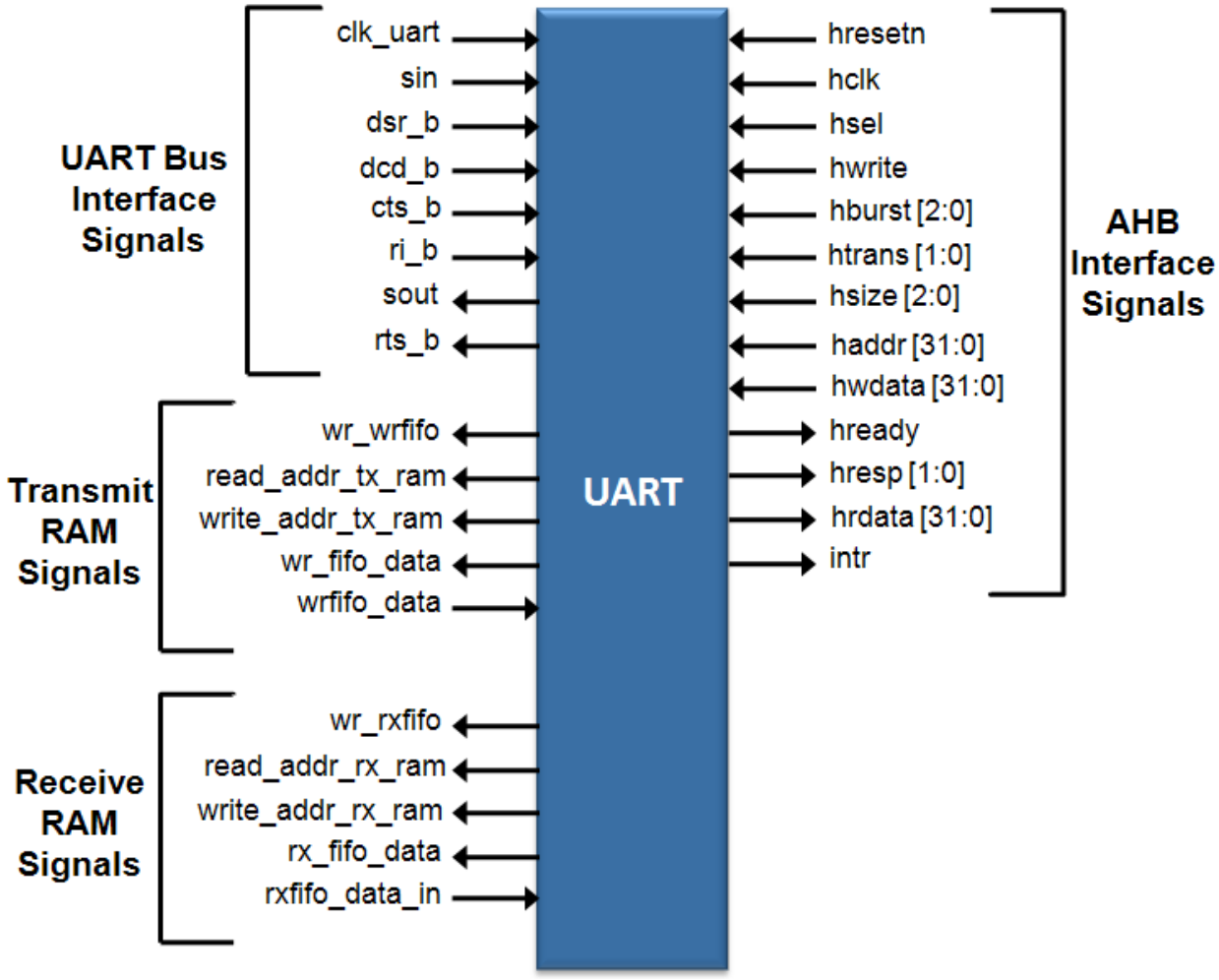


Figure 2: PIN Diagram

4 SIGNAL INTERFACES

The signal names and its descriptions used in ARASAN AHB_UART IP

- UART bus interface signals
- AHB bus interface signals
- Transmit RAM signals
- Receive RAM signals

Table 1: UART Bus Interface Signals

Pin Name	Direction	Description	Power Up Value
clk_uart	Input	UART clock	Low
sin	Input	Serial data input from MODEM	High
dsr_b	Input	Data set ready signal. Active low. RS232 interface pin when low indicates that the MODEM is ready to establish communication	High
dcd_b	Input	Active low data carrier detect signal from MODEM	High
cts_b	Input	Active low clear to send signal from MODEM	High
ri_b	Input	Active low ring indicator signal from MODEM	High
sout	Output	Serial data output to MODEM	High
rts_b	Output	Active low request to send signal to MODEM	High

Table 2: AHB Interface Signals

Pin Name	Direction	Description	Power Up Value
hresetn	Input	Active low reset	Low
hclk	Input	AHB processor clock. All signal timings are related to the rising edge of hclk	Low
hsel	Input	Slave select signal	High
hwrite	Input	When high, this signal indicates a write transfer and when low a read transfer	Low
hburst[2:0]	Input	Indicates if the transfer forms the part of the burst. Four eight and sixteen beat bursts are supported. The burst may be either incrementing and wrapping	Low
htrans[1:0]	Input	Indicates the type of current transfer which can be non sequential, sequential, idle or busy	Low
hsize[2:0]	Input	Indicates the size of the transfer which is typically byte, half word or word	Low

Pin Name	Direction	Description	Power Up Value
haddr[31:0]	Input	The 32 bit system address. This signal is routed to the AHB target core	Low
hwdata[31:0]	Input	The write data bus is used to transfer data from master to the bus slave during write operation	Low
hready	Output	When high this signal indicates the transfer has finished on the bus. This signal is driven low to extend the transfer	High
hresp[1:0]	Output	The transfer response provides additional information on the status of the transfer, OKAY, ERROR, RETRY or SPLIT	Low
hrdata[31:0]	Output	The read data bus is used to transfer the data from bus slave to the bus master	Low
intr	Output	Interrupt	Low

Table 3: Transmit RAM Signals

Pin Name	Direction	Description	Power Up Value
wr_wrfifo	Output	Write enable signal to transmit RAM	Low
read_addr_tx_ram	Output	Read address to transmit RAM	Low
write_addr_tx_ram	Output	Write address to transmit RAM	Low
wr_fifo_data	Output	Write data to transmit RAM	Low
wrfifo_data	Input	Read data from Transmit RAM	Low

Table 4: Receive RAM Signals

Pin Name	Direction	Description	Power Up Value
wr_rxfifo	Output	Write enable signal to receive RAM	Low
read_addr_rx_ram	Output	Read address to receive RAM	Low
write_addr_rx_ram	Output	Write address to receive RAM	Low
rx_fifo_data	Output	Write data to receive RAM	Low
rxfifo_data_in	Input	read data from receive RAM	Low

5 SoC LEVEL INTEGRATION

5.1 Verification Environment

This section displays the UART RTL verification and test environment.

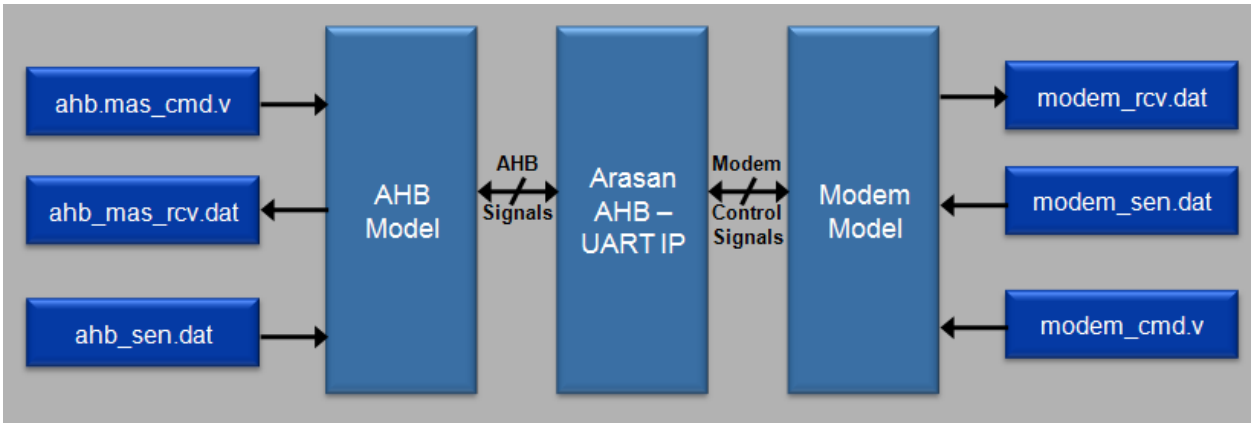


Figure 3: UART Verification Environment

5.2 IP Deliverables

The IP package consists of the following:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

6 RELATED PRODUCTS

- I2S Controller
- I2C Controller
- SPI