DATASHEET

I2C Controller

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1 INTRODUCTION

The synchronous I2C interface is a block that interconnects an APB bus to an I2C bus. The APB – I2C Bridge interfaces to the APB bus on the system side and the I2C bus on the peripheral side. The APB interface is used to easily integrate the Bridge Controller for any SOC implementation.

1.1 Overview

The APB – I2C is a master/slave interface that enables synchronous serial communication with the other master or slave I2C peripherals having I2C compatible interface. The controller performs the following functions:

- Parallel-to-serial conversion on data written to an internal 8bit wide, 1024 deep FIFO.
- Serial-to-parallel conversion on received data, buffering it in a similar 8-bit wide, 1024 deep FIFO.

Device states are read by the APB using status registers that reflect the completion of I2C transfers.

1.2 Features

1.2.1 12C Interface

- Compliant with I2C specification Version 2.1
- Supports a simple bi-directional 2-wire bus for efficient for inter-IC control
- Programmable as I2C Master mode
- Programmable as I2C slave mode
- Supports a Clock generation circuitry to derive I2C clock from APB clock
- Supports various operational frequencies from 100 KHZ to 400 KHZ
- 1024x8 bits register space is memory mapped to external I2C Master

1.2.2 APB Interface

- Compliant with AMBA Rev2.0 for easy integration with SOC implementations
- Supports APB bus for varying frequency range from 1 to 95MHZ
- Supports Bus mastering DMA modes
- Device states are read by periodic polling mechanism
- 1024X 8 FIFO to accelerate the data transfers from and to I2C and APB
- 1024x8 bits register space is mapped to APB memory

2 ARCHITECTURE

The figure below depicts the block diagram of the APB-I2C Bridge Controller. The block has an APB interface to read and write registers. The I2C interface in master mode initiates data transfer to the external I2C slave devices and in slave mode receives the data from the external I2C master. The I2C interface handles the serializing and de-serializing of data to the I2C interface from and to APB interface.

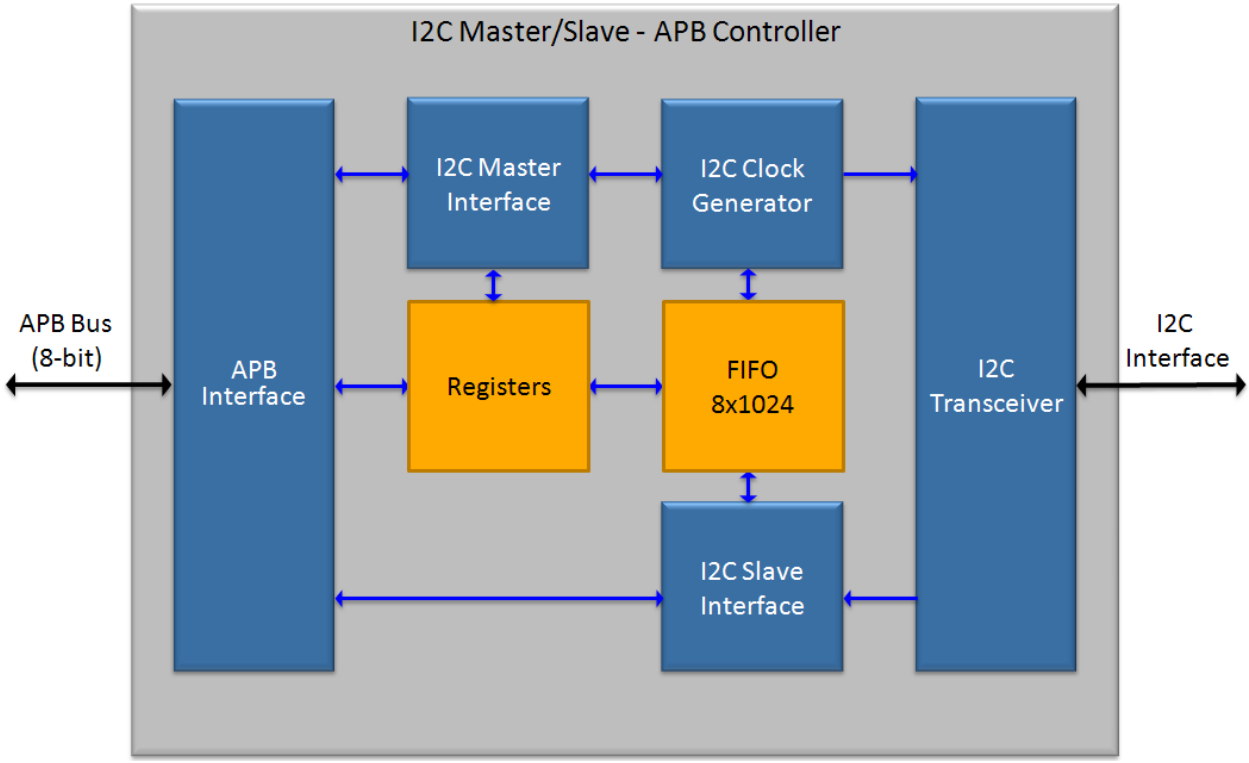

Figure 1: I2C Controller Core IP Block Diagram

2.1 APB Interface

The APB interface block is primarily used for programming the registers on the I2C controller and to transmit and receive data from the I2C master/slave devices.

2.2 I2C Master Interface

When APB - I2C IP is programmed as the I2C master interface, the APB controller initiates read and write transfers through command registers and watches the completion of the task by polling the status registers. The amount of data to be transferred or read is

predetermined by the APB controller and is programmed in the data length registers. Data to be read or written in the external I2C device is addressed using data port registers. This block throttles the data flow between the I2C interface and the APB controller in master mode.

2.3 12C Slave Interface

When the APB - I2C IP is programmed as the I2C slave interface, the APB controller polls the status register to know whether a read or write is happening in the I2C interface. When a read or write is completed the APB controller takes away the data from the FIFO by reading the data length registers and address registers to map the register locations. This block throttles the data flow between the I2C interface and the APB controller in slave mode.

2.4 I2C Clock Generator

The clock generator contains a counter. The counter is used to generated a divide signal and generate the I2C clock as required by the user by programming the divisor registers.

2.5 I2C Transceiver

The transmit and receive logic contains the state machines to receive and send data in the I2C protocol format.

2.6 Registers

The operational registers are used to program the controller and also hold status. The registers are programmed using the APB interface block and are used by the I2C controller to control the I2C interface.

2.7 FIFO

This FIFO is 8-bit wide and 1024 bit deep. It is filled by the APB controller and sent to the external I2C device by the I2C controller during a transmit operation. The same FIFO is filled by the I2C controller and read by the APB controller during a receive operation.

3 SIGNAL INTERFACES

This section describes signal names and its descriptions used in APB I2C interface

- I2C interface signals
- APB interface signals
- RAM signals
- Scan signals

Table 1: I2C Interface Signals

Pins	Direction	Description	Power Up Value
scl_in	Input	This input drives the clock from the serial EEPROM	High
sda_in	Input	This input signal is used to transfer address and data serially from the EEPROM	High
i2c_clk	Input	This input signal is generated from test_env and is used as clock for I2C interface only during master mode	High
scl_out	Output	This output drives the clock to the serial EEPROM	High
sda_out	Output	This output signal is used to transfer address and data serially to the EEPROM	High
sda_out_en	Output	This output signal is used as output enable to SDA line	High
scl_out_en	Output	This output signal is used as output enable to SCL line	High

Table 2: APB Interface Signals

Pins	Direction	Description	Power Up Value
preset_n	Input	Active low reset	Low
pwdata[7:0]	Input	Input 8 bit data bus	Low
paddr [7:0]	Input	Input 8 bit address lines	Low
penable	Input	Input processor Enable data lines	Low
psel	Input	Input processor select same as chip select	Low
pwrite	Input	Input write Enable	Low
pclk	Input	Input APB processor clock. This is also used as a reference clock for the SEEPROM interface	Low
prdata [7:0]	Output	Output 8 bit data bus	Low
inta	Output	Interrupt pin	Low

Table 3: RAM Signals

Pins	Direction	Description	Power Up Value
dataa_ram_out[31:0]	Input	Input 32 bit data bus to I2C	Low
datab_ram_out[31:0]	Input	Input 32 bit data bus to APB	Low
addressa[4:0]	Output	5 bit address lines from I2C	Low
addressb[4:0]	Output	5 bit address lines from APB	Low
dataa_ram_in[31:0]	Output	32 bit data bus from I2C	Low
datab_ram_in[31:0]	Output	32 bit data bus from APB	Low
wren_a	Output	Write enable signal from I2C	Low
wren_b	Output	Write enable signal from APB.	Low
out_en_a	Output	RAM enable signal for read from I2C	Low
out_en_b	Output	RAM enable signal for read from APB	Low
port_sel_a	Output	Port selection signal for read and write from I2C	Low
port_sel_b	Output	Port selection signal for read and write from APB	Low

Table 4: Scan Signals

Pins	Direction	Description	Power Up Value
scan_clk	Input	Input scan clock for scan operation for master interface	Low
scan_en	Input	Input signal is used to enable scan operation for master interface	Low

4 SoC LEVEL INTEGRATION

4.1 Verification Environment

This section displays the RTL verification and test environment.

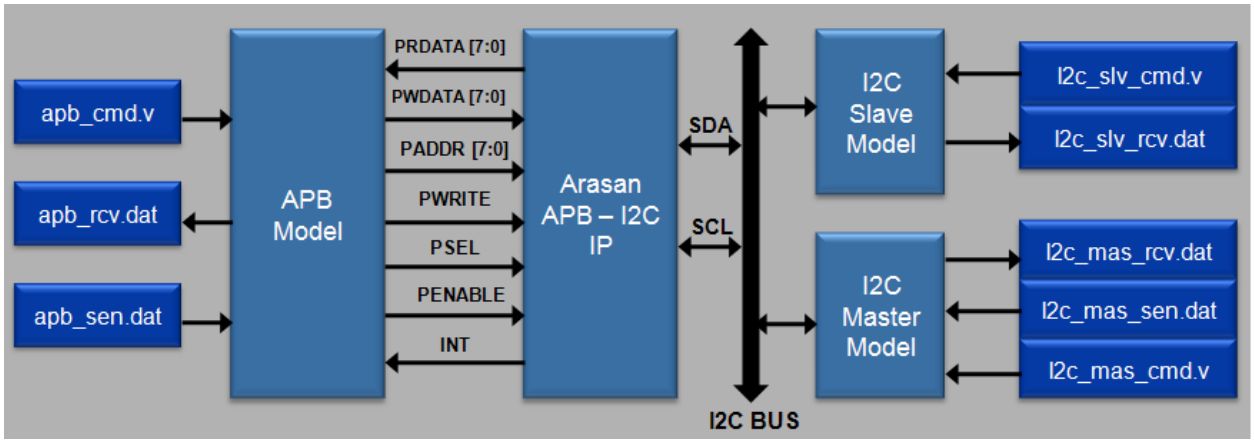

Figure 2: 12C Verification Environment

4.2 IP Deliverables

The IP package consists of the following:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents
- Simulation scripts

5 RELATED PRODUCTS

- I2S Controller
- SPI_AHB