Datasheet

I3C Total IP Solution

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1 Introduction

1.1 Arasan's Total IP Solution – Gain from our Leadership

Arasan provides a Total IP Solution, which encompasses all aspects of IP development and integration, including analog and digital IP cores, verification IP, software stacks & drivers, and hardware validation platforms. Benefits of Total IP Solution:

- Seamless integration from PHY to Software
- Assured compliance across all components
- Single point of support
- Easiest acquisition process (one licensing source)
- Lowest overall cost including cost of integration
- Lowest risk for fast time to market

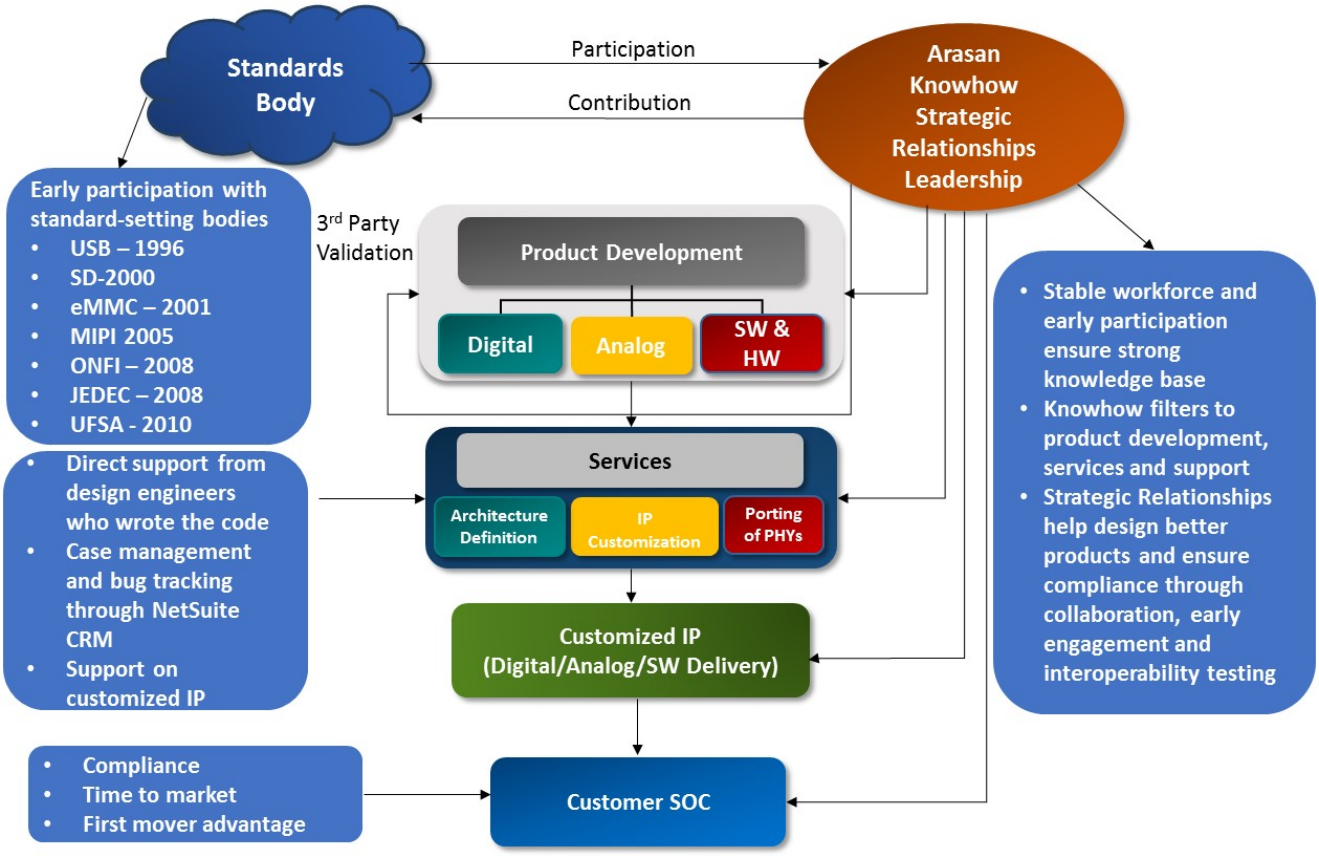

Figure 1: Arasan's Total IP Solution

1.2 Arasan's Leadership in Mobile Storage

Arasan is a leading provider of IP for the Mobile Storage Market with the launch of its SD Card IP in 2000, followed by the Multimedia Card (MMC & eMMC) in 2001 and NAND Flash Controllers in 2002. Arasan joined the ONFI Association upon its inception in 2006 and has been offering ONFI compliant NAND Flash Controllers since then.

Arasan's mobile storage IPs are silicon proven and in production with most leading Smartphone APs and Solid State Storage Devices. Being a member of MIPI since inception, Arasan has provided IP solutions to customers worldwide.

1.3 Arasan's Total IP Solution for I3C

Arasan's Total IP Solution for I3C (previously called SenseWire) comprises of the I3C Master Controller, the I3C Slave Controller and a low-level software driver (to be defined after MIPI's HCI definition for I3C has been finalized).

2 I3C Master Controller IP

2.1 Overview

The Arasan I3C Master Controller IP implements Master functionality as defined by the MIPI Alliance's I3C Specification. The I3C bus is used for various sensors in the mobile/automotive system where the Master transfers data and control between itself and various sensor devices. The I3C Master Controller IP Core provides an 8-bit AHB bus as the application interface to configure and control the I3C Master Controller IP Core. The I3C Master Controller IP can be easily integrated into an SOC to provide the required I3C functionality. Also the I3C Master Controller IP provides direct signaling to connect to the IO Buffers (SCL and SDA). Please note, that the user needs to provide appropriate IO buffers to meet the I3C specification.

The I3C Master Controller implements support for legacy I2C Slave devices, Clock frequency scaling, Open-drain and Push-pull operation of I3C Interface, and Dynamic Addressing support. The I3C Master Controller supports the required SDR mode with Clock frequency of up to 12.5 MHz and also the three HDR modes as defined by the I3C Specification. The included 16 byte FIFO (Configurable) is used to handle data transfers between IP and the external Slave Devices.

2.2 Features

- Compliant with MIPI I3C Specification V1.0
- Supports up to 12.5 MHz operation using Push-Pull.
- Open-Drain and Push-pull type transactions (as required)
- Supports legacy I2C devices.
- Dynamic Addressing while supporting Static Addressing for Legacy I2C devices
- Legacy I2C Messaging
- I2C-like Single Data Rate Messaging (SDR)
- Optional High Data Rate Messaging Modes (HDR)
- Support for Multi-master (transferring the ownership of the bus to a Secondary Master if Present).
- Reception of In-band Interrupt Support from the I3C Slave devices
- Reception of Hot-Join from newly added I3C Slave devices.
- Synchronous Timing Support and Asynchronous Time Stamping.
- AHB Target Interface for Configuring/Controlling the IP with Interrupt output.
- Small 16-byte (Configurable) FIFO for transferring data between Master and the Slave devices.
- Independent Clocks for AHB and the I3C Interface.

2.3 I3C Master Block Diagram

The following figure shows the Block Diagram of the I3C Master Controller IP and the following describes a brief overview of various Blocks inside the IP.

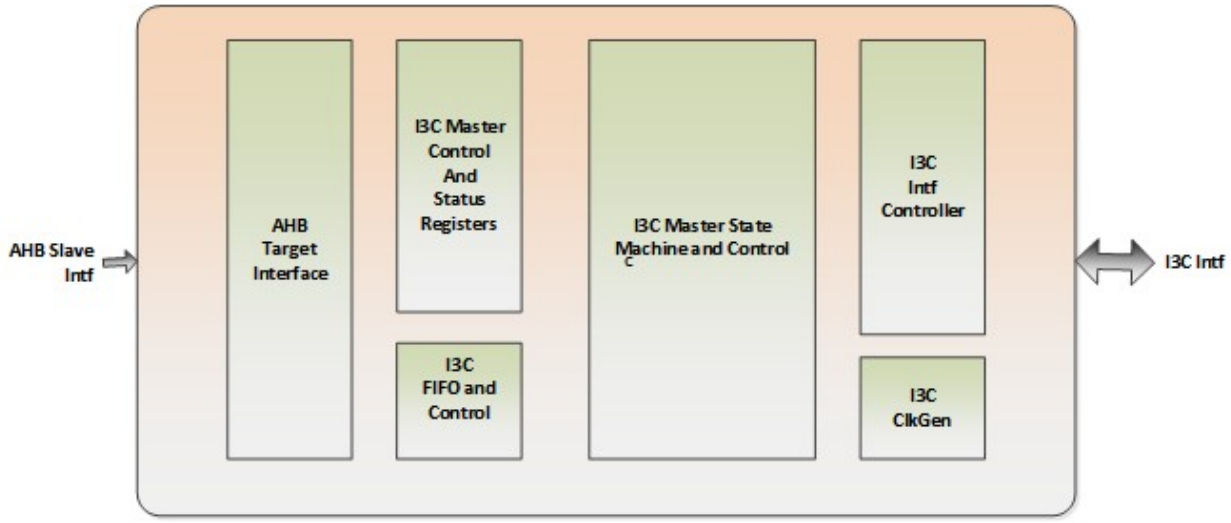

Figure 2: I3C Master Controller Block Diagram

2.4 Functional Block Diagram Description

The following provides high-level overview of various modules implemented in the I3C Master Controller.

AHB Target Interface

This module implements the AHB Target Interface Logic. This target interface supports an 8-bit data interface. The External AHB Master can use this interface to configure and control the I3C Master Controller. Also, the I3C Master controller drives Interrupt output on this interface that the external AHB Master can use for transaction controls.

I3C Control and Status Registers

This module implements the Configuration, Control and Status Registers and Data FIFO interface Registers that are accessible thru the AHB Target Interface. This module implements the Interrupt generation logic to the AHB Interface based on the enabled Interrupts (FIFO Status, or transaction completion). An access to the Data FIFO using the Data Port Registers is also provided.

I3C FIFO and Control:

This module implements the Data FIFO used for transaction transfer between the Host and the I3C Device. This FIFO is also used to return the I3C slave information during the Dynamic Address configuration and certain CCC Commands.

I3C Clock Gen

This module generates I3C Clock (SCL) from the I3C Reference Clock. The ratio of the SCL can be programmed thru the Registers. Also the I3C Master state machine will use this module to scale the SCL during certain transactions.

I3C Master State Machine

This module implements the main I3C Master state machine. Based on the AHB Register controls, various transactions are generated. This include generation of CCC commands, Read/Write data transfer commands etc.

I2C Interface Controller

This module generates the Open-Drain Vs Push-pull and the IO Controls during the transactions.

2.5 Interfaces

The I3C Master Controller IP implements the following Interfaces:

AHB Target Interface

This Interface implements the AHB Compliant Target Interface. This is used by external Application to configure and Control the I3C Controller. Also This Interface can be used to transaction data to/from the FIFOs. This interface supports only Single transaction (Non-BURST)

I3C Interface

This is a serial I3C Interface with Clock (SCL) and data (SDA). The IP provides IO buffer controls so these can be connected to external IO Pads. The controls includes Push-Pull and Open-Drain.

2.6 Signal Descriptions

2.6.1 I3C Master Controller IP Pinout Diagram

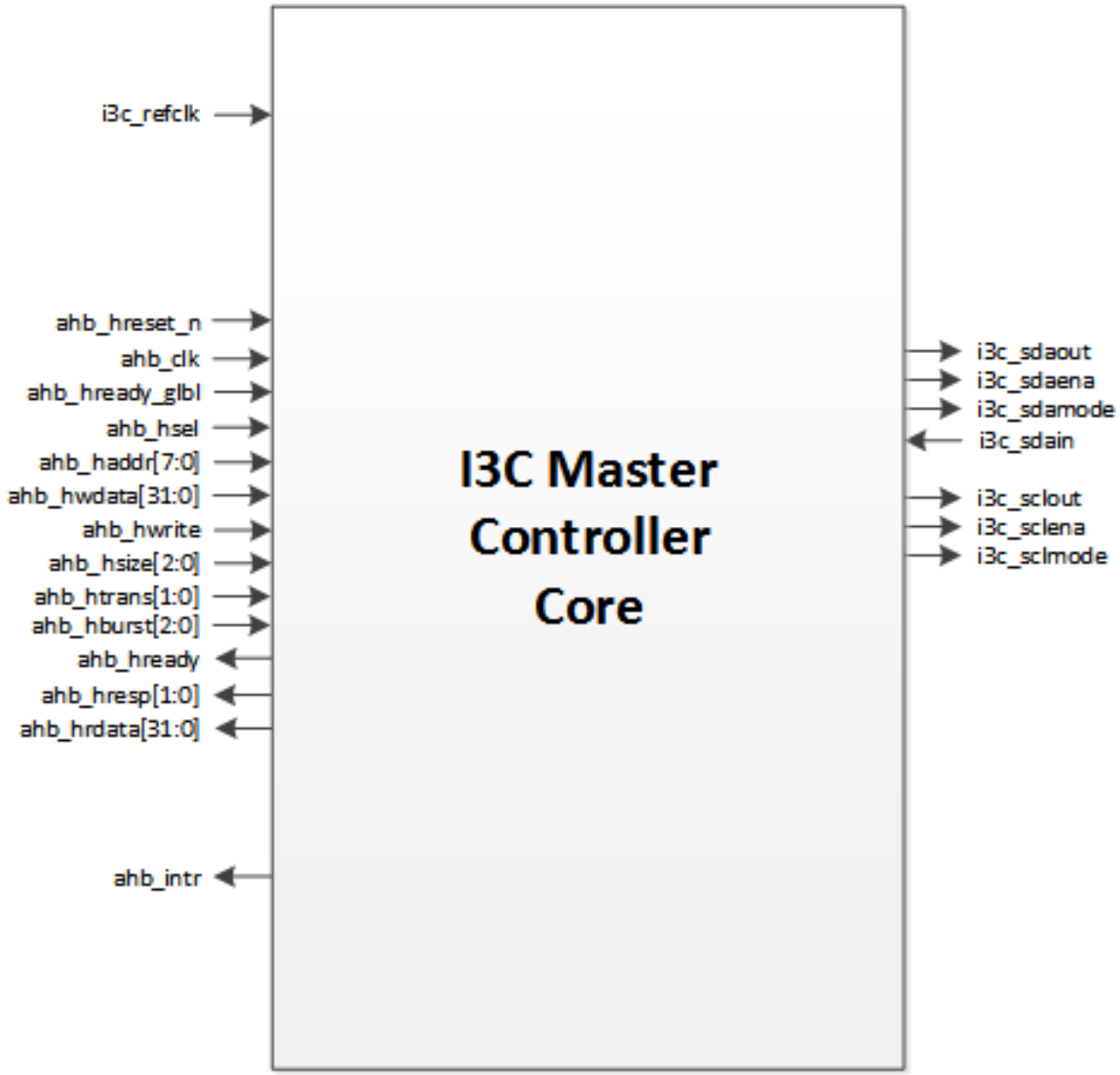

Figure 3: I3C Master Controller IP Pinout Diagram

2.6.2 I3C Master Controller Signal Description

Table 1: I3C Master Controller IP Signal Description

Signal Name	Direction	Description
a. Reference Clock		
i3c_refclk	Input	I3C reference clock. This is the reference clock on used to generate SCL. The ratio of the SCL w.r.to this clock is programmed in the Clock configuration register. This clock has to be some multiple of the SCL and at least twice the frequency of the maximum SCL. To support the maximum data rate of 12.5 MHz on the I3C Interface, this clock has to be at least 25 MHz.
b. AHB Target Signals		
ahb_clk	Input	AHB Clock: This is the clock for the AHB Bus Interface. All the AHB Interface Signals are synchronous to rising edge of this clock.
ahb_hreset_n	Input	AHB Reset: This is the reset signal synchronous to the AHB Clock. This is the global reset that resets all the logic inside the Controller. The signal is synchronized to various clock domains inside the Controller to reset the corresponding logic.
ahb_hsel	Input	AHB Select: This is the HSEL signal on the AHB Interface. When asserted, it indicates the start of transaction.
ahb_hready_glbl	Input	AHB HReady (Global). This is the HREADY signal on the AHB Interface as input. This is used to determine if any other slave has back pressured or not.
ahb_haddr [7:0]	Input	AHB Address: This is the address on the AHB Bus. The address is byte address.
ahb_hsize [2:0]	Input	AHB Size: This determines the Size of transaction (Byte, Halfword, Dword Etc).
ahb_htrans [1:0]	Input	AHB HTrans: This determines the transaction type for AHB Transfer.
ahb_bburst [2:0]	Input	AHB Burst: This determines the length and type of Burst.
ahb_hwrite	Input	AHB Write Strobe. This is the HWRITE signal on the AHB Bus. This indicates that the current transaction is a write transfer.

ahb_hwdata [31:0]	Input	AHB Write Data: This is the Write data on the AHB Bus. This is valid when the ahb_hwrite is asserted.
ahb_hready	Output	AHB Ready: This is the Ready Indication from the I3C Master Controller acknowledging the current read/write transfer. In case of Read, the Read data will be valid on ahb_hrdata bus.
ahb_hrdata [31:0]	Output	AHB Read Data: This is the Read Data on the AHB Bus. This is valid for read transactions when the ahb_hready is asserted.
ahb_intr	Output	AHB Interrupt: This is the Interrupt signal onto the AHB Bus.
c. I3C Interface		
I3c_sdaout	Output	SDA Out. This is the output for the SDA Pin.
I3c_sdaena	Output	SDA Enable. This is the SDA Enable
I3c_sdamode	Output	SDA Mode. SDA Mode. 0: Open-Drain, 1-Push-pull
I3c_sdain	Input	SDA In. This is the input from the SDA Pin
I3c_sclout	Output	SCL Out. This is the output for the SCL Pin.
I3c_sclena	Output	SCL Enable. This is the SCL Enable
I3c_sclmode	Output	SCL Mode. SCL Mode. 0: Open-Drain, 1-Push-pull

2.7 Deliverables

- RMM compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents
- Validated with 3rd Party UVM-based Slave VIP and available as an additional option

3 I3C Slave Controller IP

3.1 Overview

The Arasan I3C Slave Controller IP Implements Slave functionality as defined by the MIPI Alliance's I3C Specification. The I3C bus is used for various sensors in the mobile/automotive system where an I3C Master transfers data and control information between itself and various sensor devices. The I3C Slave Controller IP can be easily integrated into the Sensor/Slave devices with minimal gate count.

The I3C Slave Controller is highly configurable (synthesis time) to provide an optimal solution based on the Device's requirements. This include, acting as a legacy I2C device, Support for Dynamic Address Assignment, HDR (any of the three defined HDR Modes) and a configurable FIFO for data transfers. In addition, Optional I3C Slave functions like Interrupt generation, Hot-Join request generation and advanced slave with secondary master capabilities can be configured for more complex slaves. The I3C Slave Controller IP provides direct signaling to connect to the IO Buffers (SCL and SDA). Please note that the user needs to provide appropriate IO buffers to meet the I3C specification.

3.2 Features

- Compliant with MIPI I3C Specification Rev 1.0
- Supports up to 12.5 MHz operation using Push-Pull.
- Open-Drain and Push-pull type transactions (as required)
- Acts as a legacy I2C Slave while supporting Legacy I2C Messaging and protocol.
- Participates in Dynamic Addressing while supporting Static Addressing for Legacy I2C mode
- I2C-like Single Data Rate Messaging (SDR)
- Optional High Data Rate Messaging Modes (HDR) (Synthesis time configuration)
- Optional support
    - Secondary Master function.
    - Transmission of In-band Interrupt
    - Hot-Join Request Generation
- Synchronous Timing Support and Asynchronous Time Stamping.
- APB Target Interface for Configuring/Controlling the IP with Interrupt and for Data transfers.
- Small 16-byte (Configurable) FIFO for transferring data Slave Controller and the Application
- Independent Clocks for APB and the I3C Interface.
- Direct FIFO Data Transfer support for simple applications where APB Interface is not required.

3.3 I3C Slave Controller IP Block Diagram

The following figure shows the Block Diagram of the I3C Slave Controller IP and the following describes a brief overview of various Blocks inside the IP.

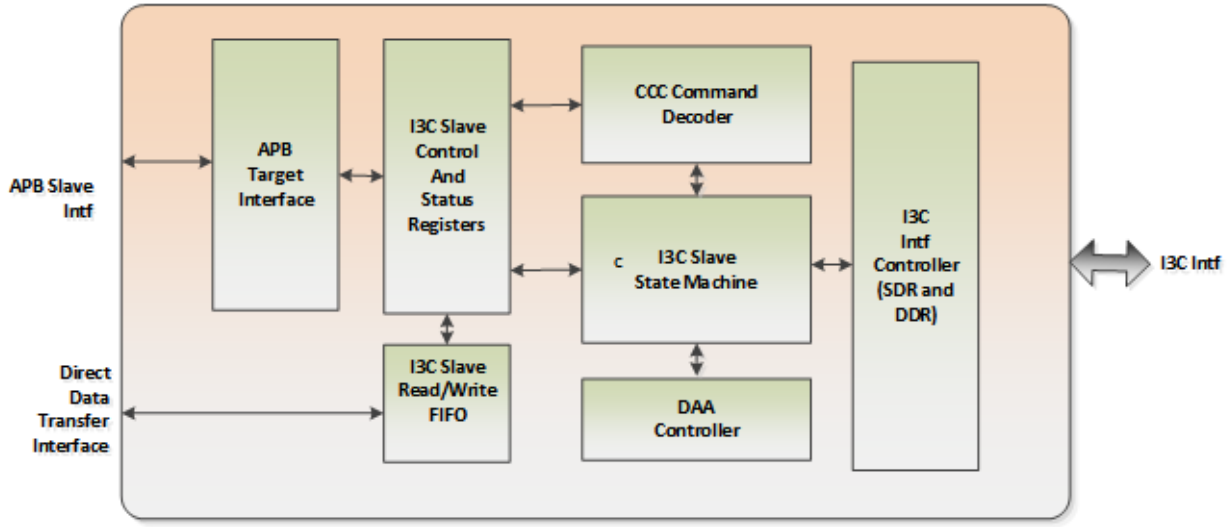

Figure 4: I3C Slave Controller Block Diagram

3.4 Module Descriptions

The following provides high-level overview of various modules implemented in the I3C Slave Controller.

- **APB Target Interface**: This is an optional Interface for advanced devices that wants to configure the Slave controller registers. This module implements the APB Target Interface Logic. This target interface supports an 8-bit data interface. The External APB Master can use this interface to configure and control the I3C Slave Controller. Also, the I3C Slave controller drives Interrupt output on this interface that the external APB Slave can use for transaction controls.
- **I3C Control and Status Registers**: This module implements the Configuration, Control and Status Registers and Data FIFO interface Registers that are accessible thru the APB Target Interface. This module implements the Interrupt Generation logic to the APB Interface based on the enabled Interrupts (FIFO Status, or transaction completion). Access to the Data FIFO using the Data Port Registers is also provided.

  The registers can be hard coded or can be driven from external input for simple slaves

- **I3C Slave Read/Write FIFO**: This module implements the Data FIFO used for transaction transfer between the Application and the I3C Slave Controller. The data from the FIFO can

be outputted directly to Application (without the use of APB Interface) or can be routed via APB Registers for interrupt driven data transfers.

- **I3C Slave State Machine**: This module implements the main I3C Slave state machine. Based on the Register controls, various transactions are decoded and optionally Slave generated transactions are generated (Interrupt, Hot Join request) etc.
- **I3C CCC Command Decoder:** This module decodes the CCC Commands and provides appropriate responses or updates the Application/registers.
- **I3C DAA Controller**: This module supports the Dynamic Address Assignment protocol and returns the required 48-bit Provision ID and the BCR/DCR registers and accepts the assigned Dynamic Address.

3.5 Interfaces

The I3C Slave Controller IP implements the following Interfaces:

- **APB Target Interface**: This Interface implements the APB Compliant Target Interface. This is used by external Application to configure and Control the I3C Controller. Also This Interface can be used to transaction data to/from the FIFOs. This interface supports only Single transaction (Non-BURST)
- **Direct FIFO Interface**: This is used to transfer data between the Application logic and the Slave controller for simple data transfers (with out the APB functionality).
- **I3C Interface**: This is a serial I3C Interface with Clock (SCL) and data (SDA). The IP provides IO buffer controls so these can be connected to external IO Pads. The controls including Push-Pull and Open-Drain.

3.6 Signal Descriptions

The following figure shows the Pinouts of the I3C Slave Controller and following table describes the individual signals. The Signals are grouped based on the associated Interface.

3.6.1 I3C Slave Controller IP Pinout Diagram

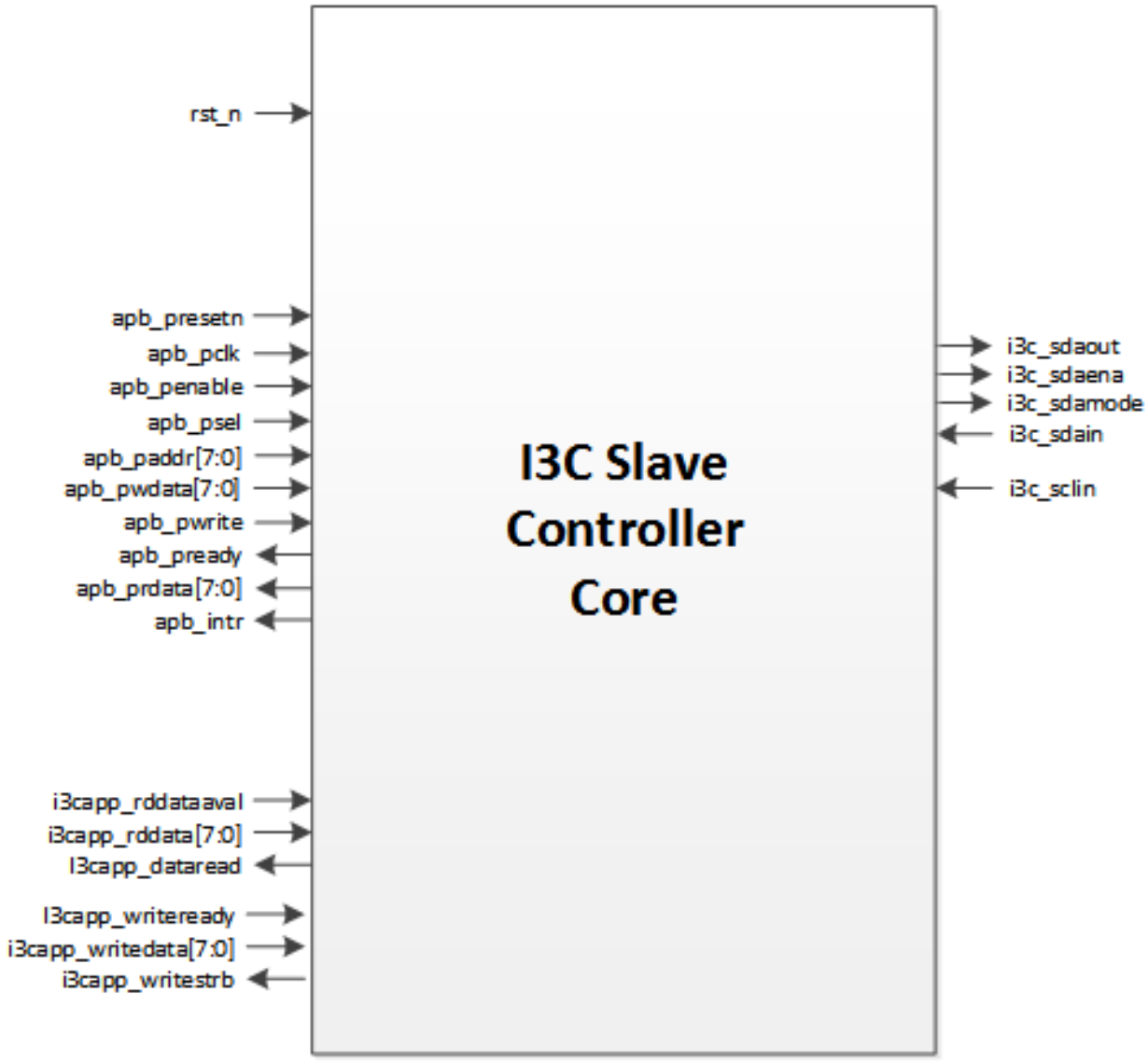

Figure 5: I3C Slave Controller IP Pinout Diagram

3.6.2 I3C Slave Controller IP Signal Description

Signal Name	Direction	Description
a. IP Configuration Signals		
corecfg_hdrcapable	*Input*	HDR Capablity
corecfg_offlinecapable	*Input*	Offline Capable
corecfg_ibipayload	*Input*	IBI Payload Present
corecfg_ibireqcapable	*Input*	IBI Request Capable
corecfg_maxspeedlimit	*Input*	Max Speed Limitation
corecfg_devchar [7:0]	*Input*	Device Characteristics (DCR Register)
corecfg_lvrcodes [3:0]	*Input*	LVR Codes in LVR Register
corecfg_i2cstaticaddr [6:0]	*Input*	I2C Static Address Value (when the value is non-zero).
corecfg_provid [47:0]	*Input*	Provision ID Inputs to be used in the DAA procedure [47:33] MIPI Mfg ID [32] Prov ID Selector (1'b1: Random, 1'b0: Vendor Fixed) [31:16]: Part ID (When using Vendor Fixed) [15:12]: Instance ID (when using Vendor Fixed) [11:0] Additional info.
corecfg_hdrcapabilities [7:0]	*Input*	HDR Capabilities from HDR Mode#0 to #7. Based on these bits, the logic to support the corresponding HDR Mode is enabled. Also this information is passed to the Master vial GETHDRCAP command.
a. System Interface		
rst_n	*Input*	**Rst_n**. This is the Power On Reset for the I3C Slave Controller. This is used to reset all the I3C Slave Controller

		logic.
b. APB Target Interface Signals		
apb_pclk	*Input*	**APB Clock**. This is the Clock on which the APB Interface operates on. All the APB Interface Signals are synchronous to rising edge of this clock.
apb_preset_n	*Input*	**APB Reset**. This is the reset signal synchronous to the APB Clock. This is the global reset that resets all the logic inside the Controller (APB Interface Logic and the Registers Logic). The signal is synchronized to various clock domains inside the Controller to reset the corresponding logic (ORed with Rst_n).
apb_psel	*Input*	**APB Select**. This is the PSEL signal on the APB Interface. When asserted, it indicates the start of transaction.
apb_penable	*Input*	**APB PEnable.** This is the PEANBLE signal on the APB Interface as input.
apb_paddr [7:0]	*Input*	**APB Address**. This is the address on the APB Bus. The address is byte address.
apb_pwrite	*Input*	**APB Write Strobe**. This is the PWRITE signal on the APB Bus. This indicates that the current transaction is a write transfer.
apb_pwdata [7:0]	*Input*	**APB Write Data**. This is the Write data on the APB Bus. This is valid when the *apb_hwrite* is asserted.
apb_hready	*Output*	**APB Ready**. This is the Ready Indication from the I3C Slave Controller acknowledging the current read/write transfer. In case of Read, the Read data will be valid on *apb_prdata* bus.
apb_prdata [7:0]	*Output*	**APB Read Data**. This is the Read Data on the APB Bus. This is valid for read transactions when the *apb_pready* is asserted.
apb_intr	*Output*	**APB Interrupt**. This is the Interrupt signal onto the APB Bus.
c. I3C Interface		

i3c_sdaout	*Output*	**SDA Out**. This is the output for the SDA Pin.
i3c_sdaena	*Output*	**SDA Enable**. This is the SDA Enable
i3c_sdamode	*Output*	**SDA Mode**. SDA Mode. 0: Open-Drain, 1-Push-pull
i3c_sdain	*Input*	**SDA In**. This is the input from the SDA Pin
i3c_sclin	*Input*	**SCL Input**. This is the input for the SCL Pin.
d. Direct FIFO Interface		
i3capp_rddataavil	*Input*	**Read Data Available**. This is an indication that the Application has the Read Data Available.
i3capp_rddata[7:0]	*Input*	**Read Data**. This is the Read data for sending in I2C or I3C Slave Read Operations.
i3capp_dataread	*Input*	**Data Read Indication**. This is the Data Read Indication. The Application can use this to send the next Byte for the Slave.
i3capp_writeready	*Input*	**Write Ready**. This is an indication by the application, that the Application is ready to accept the data in the I2C/I3C Slave Write transfers.
i3capp_writedata[7:0]	*Output*	**Write Data**. This is the Write data byte that is received from the I3C Master in slave Write transaction.
i3capp_writestrb	*Output*	**Write Strobe**. This is the write strobe Indication.

Table 2: I3C Slave Controller IP Signal Description

3.7 Deliverables

- RMM compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents
- Validated with 3rd Party UVM-based Slave VIP and available as an additional option

4 Services & Support

4.1 Global Support

Arasan Chip Systems provide global support to its IP customers. The technical support is not geographically bound to any specific site or location, and therefore our customers can easily get support for design teams that are distributed in several locations at no extra cost.

4.2 Arasan Support Team

Our technical support is provided by the engineers who have designed the IP. That is a huge benefit for our customers, who can communicate directly with the engineers who have the deepest knowledge and domain expertise of the IP, and the standard to which it complies.

4.3 Professional Services & Customization

At Arasan Chip Systems we understand that no two Application Processors are the same. We realize that often the standard itself needs some tweaks and optimizations to fit your design better. Sometimes, the interface between the IP blocks and your design need some customization. Therefore, we provide professional services and customization to our IP customers. We do not sell our IP blocks as “black box” that cannot be touched. Please contact us for more details on our customization services.

4.4 Pricing & Licensing

Arasan charges a one-time licensing fee, with no additional royalties. The licensing fee gives the right to use our IP for 1 project. Licensing fee for additional projects, using the same IP, is discounted. We also offer unlimited-use license. For any additional information regarding pricing and licensing – please contact our sales at: sales@arasan.com.