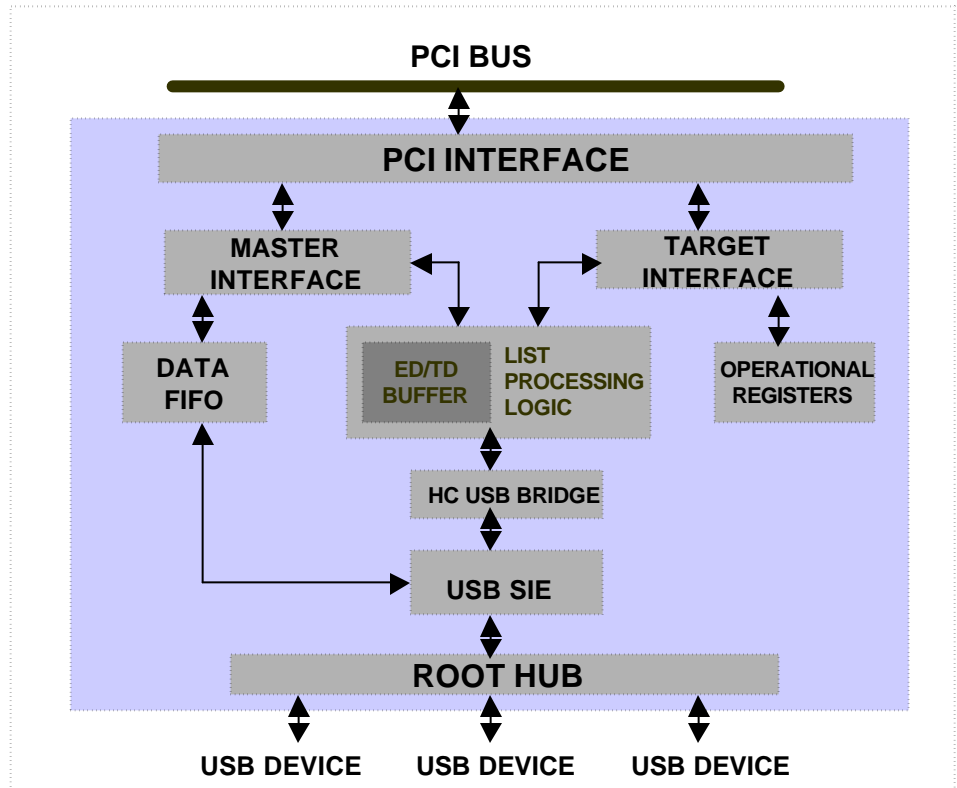


# USB1.1 Host Controller Core

## Features

- Fully compliant to the Open HCI specification
- FPGA Board proven core.
- Synthesizable VHDL/Verilog source code
- Supports asynchronous communication between host CPU and USB devices
- Supports two types of USB devices: full speed (12 Mbps) devices and low speed (1.5 Mbps) devices.
- System clock: 48 MHz
- FIFO of 32 bytes on PCI side and 2 ping pong buffers of 32 bytes each on the USB side
- 3 downstream ports
- Foundry and process independent design



## Overview

Arasan's USB1.1 host controller core interfaces the microprocessor to the USB ports. The microprocessor interface can be through AMBA, VCI, or PCI bus interfaces. The core development has been in accordance with the Reuse Methodology guidelines. The core is supported with an extensive test environment and comprehensive documentation. The core is suitable for firmware driven System On Chip projects involving USB links.

## Description

Arasan USB1.1 host controller contains the USB interface, Host controller and the PCI interface.

The USB interface contains a Serial Interface Engine (SIE) logic and the Root hub. The SIE logic is used to encode and decode the USB packets during transmission and reception respectively. The suspend and reset signaling can also be transmitted through the SIE. Root hub logic detects the connection and disconnection of devices, the speed of the connected device, and also generates information for the 3 port status registers and the root hub status register.

The Host Controller contains a logic to communicate with the USB interface (HC-USB bridge), logic to interface the core as a target to the PCI bus (Target logic), logic to interface the core as a master to the PCI bus (Master interface) and a list processing logic.

The PCI interface contains the logic to convert the data transfer requirements from the Host controller into PCI transactions in both target and master modes of operation.