DATA SHEET

MIPI® SLIMbus® Host Controller

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1 Introduction

1.1 Overview

Arasan Chip Systems is a leading SoC IP provider of a complete suite of MIPI compliant IP solutions which consist of analog PHY and digital controller IP Cores, Verification IP, Software stacks and drivers, Hardware Validation Platforms for software development and Compliance Testing, and optional customization services.

The MIPI compliant IP Cores serve as interface building blocks that simplify sub-system level interconnect architectures in mobile platforms. This leads to smaller footprint, greater interoperability between mobile IP, chips and devices from diverse sources, and lower power and EMI.

This document describes the Arasan IP Core that functions as a MIPI SLIMbus Host Controller, which typically resides in a mobile platform's application processor and provides two-wire, multi-drop connectivity with multiple audio and other Low/Mid bandwidth peripheral devices.

1.2 Features

- Compliant with MIPI SLIMbus specification version 2.0
  - Delivered in Reuse Methodology Manual (RMM) compliant Verilog RTL format
  - Small footprint
- Support for Multichannel Stream
- Support for Multiline configuration
- Contains full-featured active interface device, with support for
  - Dynamic channel allocation and management
  - All SLIMbus Core Messages
  - Error handling and recovery, as defined in the MIPI SLIMbus specification
- Embedded Framer which can be active or passive, and supports SLIMbus clock generation handoff To/From Framers in other components, with support for
  - Clock Gears 1 to 10, either as clock source or clock receiver
  - Maximum of 28.8 MHz bit-serial rate
  - Dynamic SLIMbus clock frequency scaling and clock Pause/Resume minimizes power

- Contains one generic device with up to 8 active port pairs; each port supports
    - Isochronous, Pushed, Pulled, Asynchronous Simplex, Extended Asynchronous Simplex and Locked transport protocols over SLIMbus with data segment size of 1 to 31 slots
    - Interface options to application processor
        - Generic FIFO Interface
            - Audio or peripheral data sample sizes of 8,16, 24 or 32 bits
            - Different port pairs can have different sampling rates
    - Slave DMA Interface
        - Each generic port has separate channel to external DMA master
        - Interrupt wake-up mechanism to turn system bus interface on when SLIMbus host ready to Source/Sink system memory data
    - 32 bit AHB 2.0 Slave Interface to CPU/Memory sub-system
        - System Clock frequency range from 66 to 150 MHz
        - Used by driver to configure the IP using Programmed IO
        - Optionally used for data transfer To/From generic device

2 Architecture

2.1 Functional Description

The Arasan SLIMbus Host Controller IP is designed to provide MIPI SLIMbus 2.0 compliant connectivity to a SoC.

As a SLIMbus host, this IP is responsible for the establishment, maintenance and shutdown of the entire SLIMbus system under control of the host software Drivers/Stack and in response to the presence and bandwidth requirements of the various SLIMbus devices on the bus.

SLIMbus has a TDM channel allocation structure for control messages and data. When its Framer is active, the host drives the SLIMbus clock, creates the SLIMbus frames, and enables the various devices to synchronize and share the available bandwidth.

This IP contains a configurable generic device that transfers data to and from remote SLIMbus components and the SoC's system memory. Alternately, one or more port pairs of the generic device can be used by SLIMbus host component to incorporate

bridge functions to legacy interfaces, like I2S, I2C and SPI, or interface directly to audio DAC's and ADC's.

2.2 Functional Block Diagram

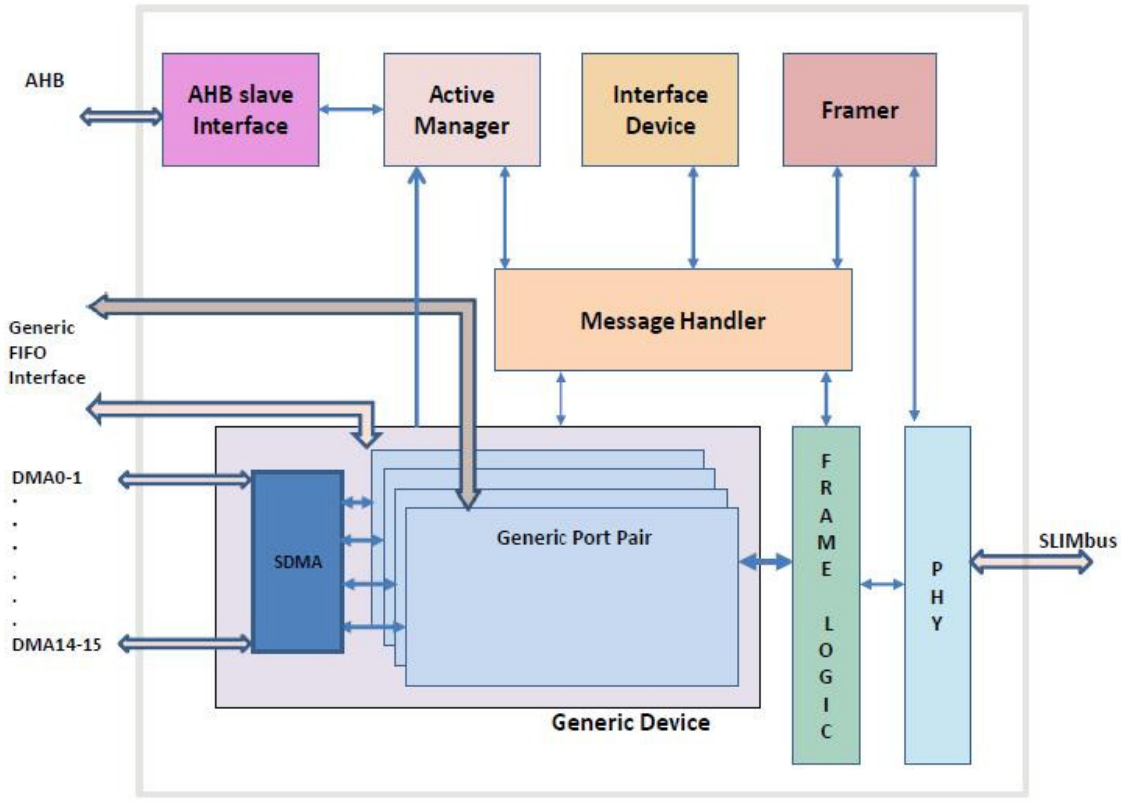


Figure 1: SLIMbus Host Functional Block Diagram

2.3 Functional Block Diagram Description

2.3.1 Slave Interface

The AHB Slave Interface block is the programming interface for the software drivers to receive and send control messages for the SLIMbus system and configures the IP through a combination of interrupts and programmed IO. In addition, this block performs data transfers To/From system memory and the IP's internal Generic Device when running in DMA mode of operation.

2.3.2 Active Manager

Active Manager is responsible for the administration of the SLIMbus namely, enumeration of the SLIMbus devices, bus configuration, and bandwidth allocation for the data channels. It communicates with the host system and the driver stack via the Slave Interface block. One Active Manager is required per SLIMbus system.

2.3.3 Interface Device

Each SLIMbus component requires one Interface Device, which provides SLIMbus management services for the component. This block manages component reset so that a component can properly sequence its devices. In addition, it reports information about the status of the component to the other SLIMbus components.

2.3.4 Framer

SLIMbus requires one Framer on the bus to be active at a given time. The SLIMbus Host IP from Arasan can function as the Active Framer for the bus, or transfer this role to another Framer on the bus. When active, the Framer is responsible for booting the SLIMbus, generating the SLIMbus clock and providing the Frame Logic block with the frame synchronization symbol, frame structure and timing information, and guide channels.

2.3.5 Message Handler

This block routes to the Active Manager, Interface Device or Framer the relevant fields of all incoming messages extracted by the Frame Logic block. It performs the opposite function for outgoing messages.

2.3.6 Generic Device

This block contains up to 8 generic data port pairs which can transfer data To/From system memory through Slave DMA. For applications which require bridging to other protocols, like I2S or I2C, or for direct interface to DAC's or ADC's, the Generic FIFO Interface is made available. Each port pair can be configured either as data source or sink with respect to SLIMbus.

2.3.7 Frame Logic

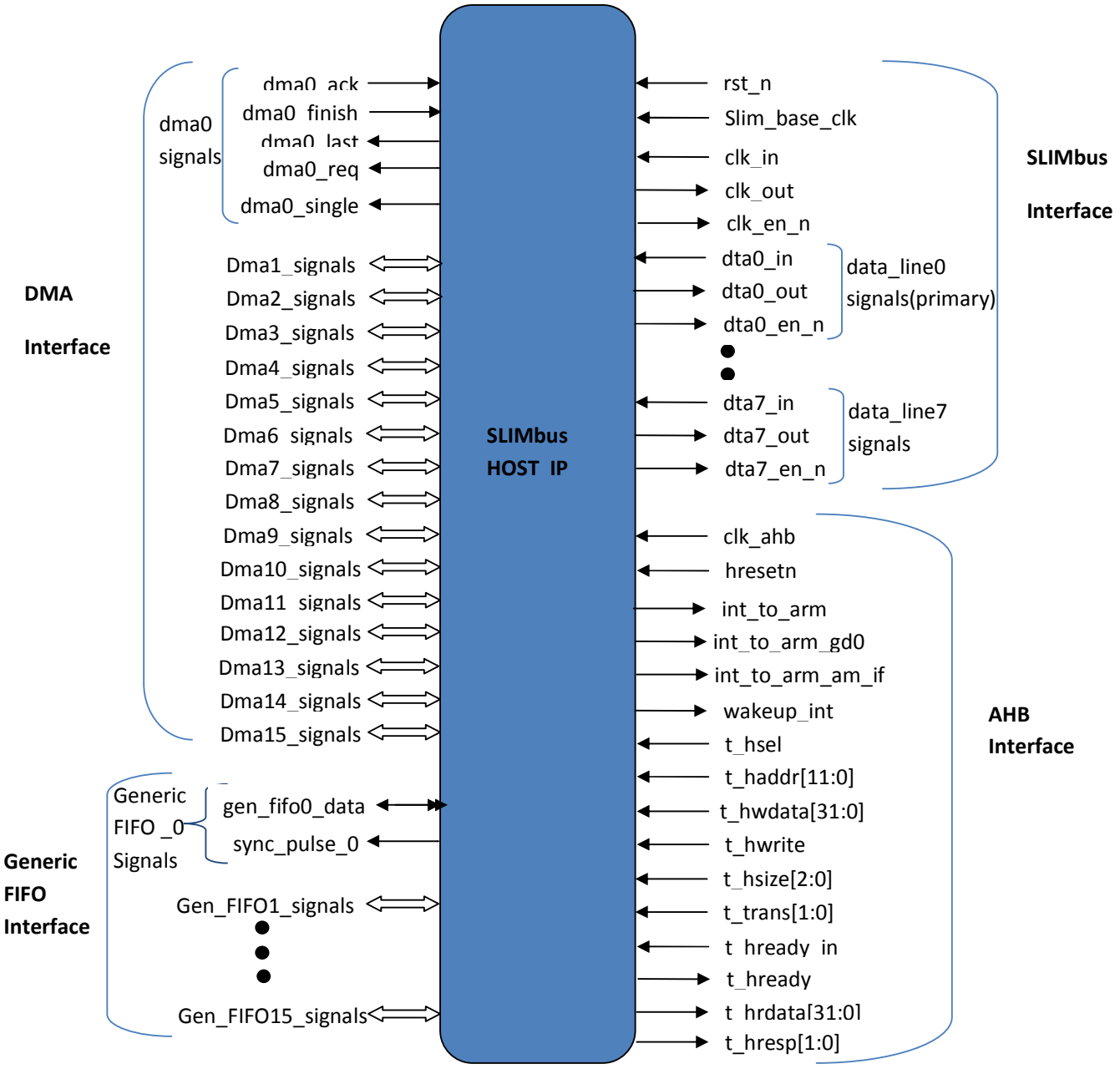
This block, which implements the Frame layer, is responsible for synchronizing with framing, guide, message and data channels. During transmission, this block interleaves control and data channels into a single, serialized bit stream to be driven by the PHY onto the SLIMbus. For incoming bit streams, this block separates the control and data streams, and routes them to the message handler and the generic device respectively.

2.3.8 PHY

The Physical layer drives and captures the bit stream between SLIMbus components. Signaling is CMOS-like, with Non-Return-to-Zero Inverted (NRZI) coding for the data lines. Data is driven on the positive edge and read on the negative edge of the SLIMbus clock. The SLIMbus Host Controller IP provides the data and Clock Input/ Output and enable signals, which allows users to choose the appropriate bidirectional pads at the chip level.

3 PIN Diagram

3.1 AHB or Generic FIFO Interface to SLIMbus Pin Diagram



- gen_fifo_data can be configured as as 8/16/24/32 bit source or sink
- sync_pulse is the synchronization signal driven by the IP

Figure 2 : SLIMbus Host Controller Pinout Diagram

4 SoC Level Integration

4.1 IP Deliverables

- Verilog HDL of the IP Core
- Synthesis scripts
- Gate count estimates available upon request
- User guide
- Verification environment and tests

4.2 Verification Environment

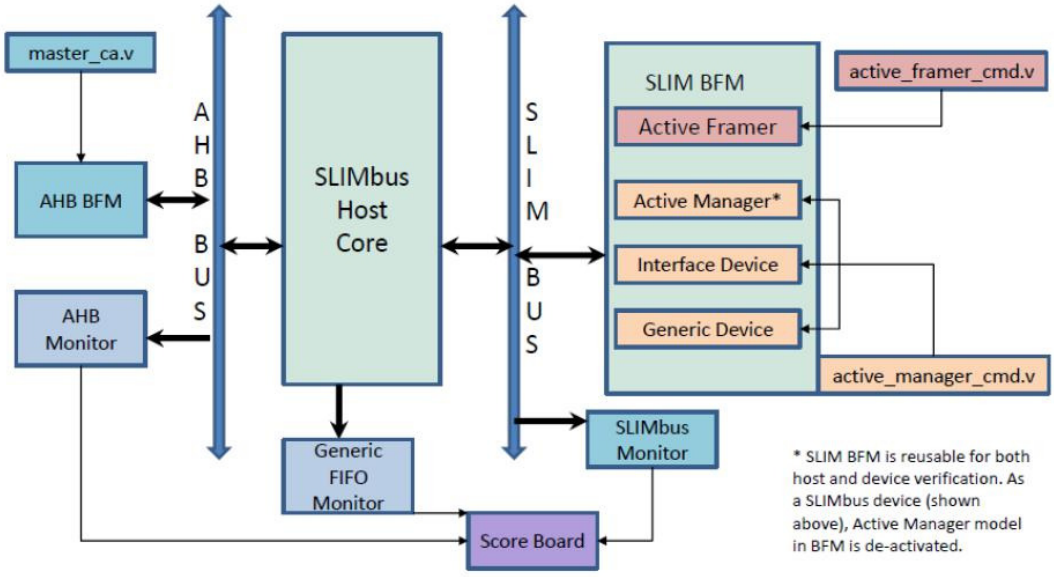


Figure 3: SLIMbus Host IP Verification Environment

- Comprehensive suite of simulation tests for ease of SoC integration
- Verification components and test files provided
- Verification environment and test suite well documented

4.2 Related Items for Total Solution

- Hardware Validation Platform
  - Standard, low profile Linux platform, with Xilinx Spartan 6 FPGA mounted on Arasan PCI-Xpress add-on card
  - FPGA contains SLIMbus Host controller, along with PCIe to AHB wrapper
  - Device driver binaries included; source software stacks sold separately

- Host Software Stack
  - Function Driver development offered as a service

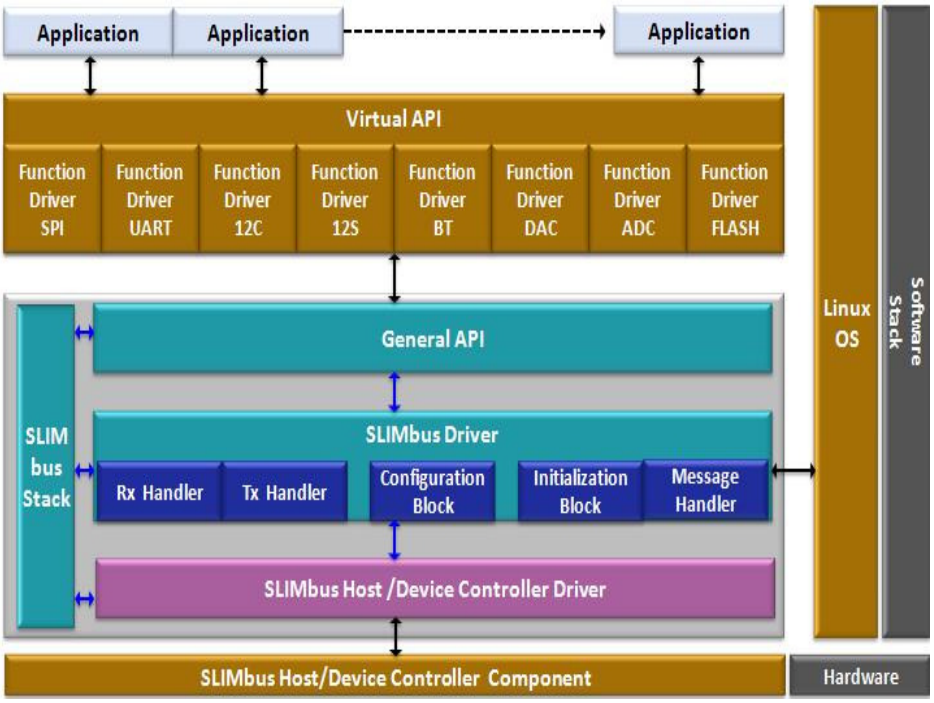


Figure 4: SLIMbus Host Software Stack

