DATA SHEET

SD 4.1 UHS-II PHY

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1 Introduction

1.1 Overview

The rapid proliferation of high-performance mobile and handheld devices has resulted in increasing requirements for non-volatile memory. Memory interfaces with larger capacities and faster access times are needed. In response to these trends, SD 4.1 (UHS-II) achieves a peak interface speed of 3.12 Gbps. Arasan's UHS-II PHY is compliant with the specification of UHS-II and is an extremely area and power efficient implementation. This interface is backward compatible with legacy SD cards. Both Host and Device UHS-II PHY configurations are available from Arasan.

The UHS-II PHY IP is a comprehensive, silicon-proven configurable core that has been ported to multiple process nodes and leading foundries. It uses sub-LVDS signaling consisting of one pair each for transmit, receive and an additional reference clock. This low-pin count interface has reduced power consumption and low Electro Magnetic Interface (EMI). To further reduce power, the reference clock operates at 1/15th or 1/30th of the data transfer speed. This differential clock operates between 26MHz to 52 MHz and is carried over the legacy SD lines DAT0, and DAT1.

Arasan's UHS-II PHY operates in both the Full-duplex and Half-duplex modes. It includes an 8b/10b encoder/decoder. The controller side of the interface of the UHS-II PHY operates in the range between 39 Mbps to 156 Mbps. The default data lane D0 is used for downstream connection and the D1 lane is used for the other direction. An 8b/10b coding scheme is used. To improve testability, the UHS-II PHY implements the standard loopback paths.

1.2 Features

The following is a top-level feature support for the Arasan MIPI® UniPro 1.6 digital IP core.

- Compliant with SD Specifications Part 1 UHS-II Specification Volume 1: System and Protocol
- Per lane data rate between 390 Mbps to 1.56 Gbps
- Supports peak interface speed of 3.12 Gbps in Half-duplex; 1.56 Gbps in Full-duplex mode
- Sub-LVDS differential PHY signaling
- Low frequency differential reference clock (1/15th or 1/30th) of data rate
- Supports Spread Spectrum clocking to reduce EMI
- Flexible transmission rates from 390Mbps - 1.56 Gbps (each lane)
- Multiple power saving modes: Dormant, Line standby
- Low power, reduced EMI operation
- Integrated solution with built-in termination, no external components required
- Easily ported to various process nodes and foundries

2 Architecture

2.1 Functional Description

The Physical Layer Interface is divided into two major sub groups called Analog Front End (AFE) and Digital Front End (DFE). The UHS-II interface utilizes transmission Lines (including socket and pins) and terminations which are meant to keep the impedance matching for high speed transmission. UHS-II interface introduces the additional pins for high speed data transmission.

UHS-II has two data Lanes. D0 and D1 Lanes are used for differential transmission between Host and Device which are dedicated to UHS-II interface only, and are separate for signals of legacy SD interface. D0 is used for downstream (from Host to Device), thus WRITE data and command are transferred from Host to Device on this Lane. However, when enabling the optional (Half duplex) 2L-HD mode, it is possible to use D0 Lane as upstream (from Device to Host). D1 is used for upstream, thus READ data and response are transferred from Device to Host on this Lane. However, when enabling the optional (Half duplex) 2 L-HD modes, it is possible to use D1 Lane as downstream. The D0 and D1 signals are encoded by 8b/10b code before transmission, and decoded by 10b/8b after receiving.

The key features of Physical Layer are defined as follows:

- Differential low voltage signaling
- Flexibility of transmission rates
- Low Frequency Reference Clock (RCLK)
- Two types of duplex mode: FD mode (mandatory), 2L-HD mode (optional)
- Additional pins for High-Speed differential transmission
- 8b/10b coding
- Enhanced power saving modes

2.2 Functional Block Diagram

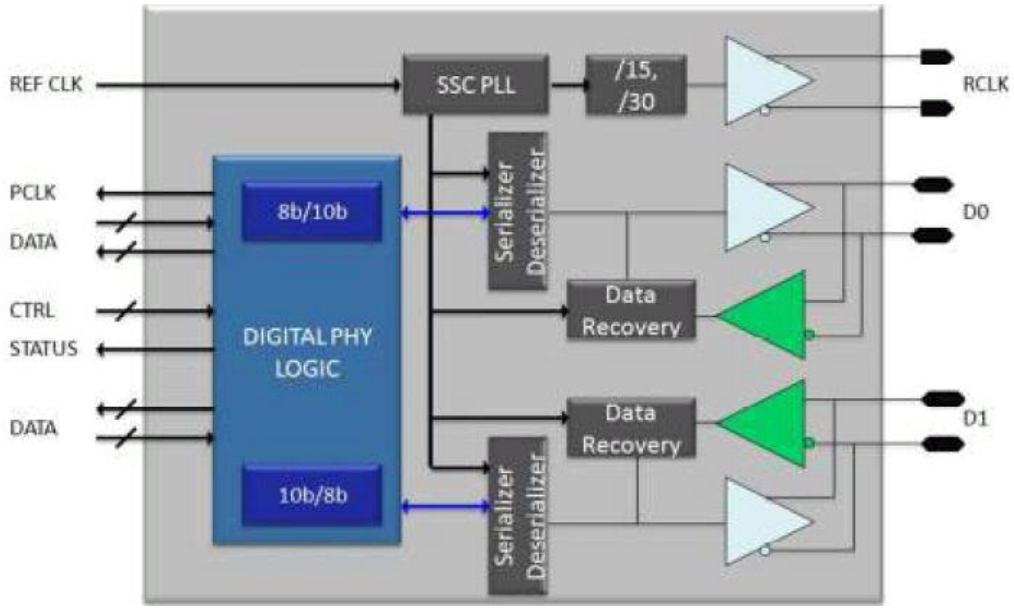

Figure 1: UHS-II PHY Functional Block Diagram

2.3 Functional Block Diagram

2.3.1 UHS II PHY

The UHS-II PHY IP is a comprehensive, silicon-proven configurable PHY that has been ported to multiple process nodes and leading foundries. Both Host and Device PHY IP are available. The Host configuration of this IP supports spread spectrum clocking that reduces EMI.

The UHS-II PHY using sub-LVDS signaling has a low pin count to reduce power consumption and EMI. The PHY supports interface speeds between 390 Mbps to 1.56 Gbps. To ease system level board design and reduce BOM, the termination resistors are included inside the UHS-II IP.

2.3.2 Data Lanes D0, D1

The high-speed data lanes D0, D1 operate in two modes: Full-Duplex (FD) and Half-Duplex (HD). In the default FD mode, D0 is used for downstream (from Host to Device), thus WRITE data and command are transferred from Host to Device on this Lane. However, when enabling the optional HD mode, it is possible to use D0 Lane as upstream (from Device to Host).

D1 is used for upstream, thus READ data and response are transferred from Device to Host on this Lane. However, when enabling the optional HD mode, it is possible to use D1 Lane as downstream. D0 and D1 Lanes are used for differential transmission between Host and Device which are dedicated to UHS-II interface only, and are

separate for signals of legacy SD interface. The D0 and D1 signals are encoded by 8b/10b code before transmission, and decoded by 10b/8b after receiving.

2.3.3 UHS-II Digital Front End PHY Logic

The Digital Front End (DFE) PHY interfaces with the Link Layer of Arasan's UHS-II Controller IP core. The DFE maintains the configuration registers, reports on status, and performs 8b/10b processing of data.

The UHS-II DFE PHY performs following operations:

- Symbol alignment
- 8b/10b encoding and 10b/8b decoding
- Support PHY initialization sequence
- Enable and disable loopback path and maintain LSS boundary before and after enabling / disabling look pack mode
- Switching between FD and HD mode per Link Layer's request

2.3.4 Reference Clock Lane (RCLK)

RCLK is transmitted from Host to Device. Whenever SD4.1 Host output a RCLK to the SD4.1 UHS-II Device, the RCLK signal frequency and phase should be stable in the frequency and phase. The RCLK shall not be stopped and its frequency shall not be changed during UHS-II transmission, even within the same range.

The RCLK frequency is lower than the lowest data rate. Therefore, the Device shall generate high frequency clock or multi-phase clocks internally for sampling the high speed data.

The RCLK frequency is in the range of 26 MHz to 52 MHz. Data rate is from 390 Mbps to 1.56 Gbps per Lane. The Card RCLK is sent through DAT0 and DAT1 lines of legacy SD3.0 interface. Thus, RCLK does not require additional pins. Card RCLK receiver shall be tolerant to single ended voltage range of 0V to 3.6V DC.

2.3.5 Power Domains

There are three power domains in this UHS-II PHY:

- VDD2 – Supplied by the Host (typically 1.8V), powering the VREG
- VDDP – Analog circuits supply voltage, generated by VREG. This supply voltage can be switched off when VREGEN=0.
- VDDD – Digital core supply voltage (typically 1.2V). Used for the digital circuits and level shifters between the domains.

2.3.6 Voltage Regulator (VREG)

The UHS-II PHY is powered by VDD2 which is typically 1.8V supply. Internal PHY circuits may operate at lower voltage named VDDP based on the process technology. The generation of the voltage is done by internal voltage regulator (VREG).

The key features required from VREG are:

- Ability to override the regulator and force external supply (for testing and Characterization).
- VDDP of the regulator should have bonding pad for external connection
- VREG is enabled when VREGEN=1

3 Signal Interfaces

The UHS-II PHY has the following interfaces:

- UHS-II PHY External Interface
- UHS-II PHY Controller Interface
- PHY, LINK and External Interface

Table 1: UHS-II PHY External Interface (UHS-II Host configuration)

Pin	Direction	Description
RCLK_p	Output	Positive polarity of low voltage differential clock signal
RCLK_n	Output	Negative polarity of low voltage differential clock signal
D0_p	I/O	Positive polarity of low voltage differential data signal of D0
D0_n	I/O	Negative polarity of low voltage differential data signal of D0
D1_p	I/O	Positive polarity of low voltage differential data signal of D1
D1_n	I/O	Negative polarity of low voltage differential data signal of D1
VDD2	Supply	1.8V input to VREG
VDDP	Supply	Output of VREG
VDDD	Supply	1.2V input from external supply
GNDA	Supply	Ground pin for analog circuits
GNDD	Supply	Ground pin for digital circuits

Table 2: PHY- LINK Interface

Name	Pin	Direction	Description
		Input LINK →PHY Output PHY→LINK	
SCLK		Input	Source clock to MUL block host
PCLK		Output	Parallel interface clock at symbol rate
RSTN		Input	Active low, asynchronous Reset
TRIM_0[31:0]	Width 32	Input	TRIM Bits for AFE
TRIM_1[31:0]	Width 32	Input	TRIM Bits for AFE

Name	Pin	Direction	Description
TRIM_2[31:0]	Width 32	Input	TRIM Bits for AFE
TRIM_3[31:0]	Width 32	Input	TRIM Bits for AFE
CT	PINIT [3:0] (when MODE = 0)	Input	[1:0] Select PHY Reserved [3:2] Select Transmission Speed Range 00: Range A (390-780 Mbps per Lane at UHS 156) 01: Range B (780-1560 Mbps per Lane at UHS 156) Others: Reserved
	PCMD[3:0] (when MODE = 1)	Input	PHY Command 0000: No Command Operation 0001: Enter to Loopback mode for DB Streaming 0011: Exit from Loopback mode for DB Streaming 0101: Enter to HDIN mode (Default Tx -> Rx) 0110: Enter to HDOUT mode (Default Rx -> Tx) 0111: Exit from HD mode 11XX: Reserved for Vendor Unique Command others: Reserved
	TDS [5:4]	Input	TD State Control 00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Standby state with fixed DIF-L or DIF-H) 11: VLD (Valid 8b/10b Symbol state with DIF-L or (DIF-H))
	TDRS [7:6]*	Input	TDR State Control 00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Standby state with fixed DIF-L or DIF-H) 11: VLD (Valid 8b/10b Symbol state with DIF-L or (DIF-H))
RD	Width 8 or 16	Output	Receive Data of Rx Block
RDM	Width 1 or 2	Output	RD Coding Mode (0: D-Symbol, 1:K-Symbol)
RDT*	Width 8 or 16	Output	Receive Data of Tx Block
RDTM*	Width 1 or 2	Output	RDT Coding Mode (0: D-Symbol, 1:K-Symbol)
ST	ST(0:3)	Output	PHY Status

Name	Pin	Direction	Description
			[0]: DET Amplitude Detector Output (high active) [1]: LOCK PLL Lock (high active) [2]: PACK PCMD acknowledge (high active) [3] ERR PHY Receive Error Status (0: No Error, 1: Error occurs on at least one data Lane
	RDS (5:4)	Output	RD Status 00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Invalid 8b/10b Symbol state with DIF-L or (DIF-H)) 11: VLD (Valid 8b/10b Symbol state with DIF-L or (DIF-H))
	RDTS(7:6)*	Output	RDT Status 00: EIDL (Electrical Idle state with DIF-PD) 01: OFF (Electrical Off state with DIF-Z) 10: STB (Invalid 8b/10b Symbol state with DIF-L or (DIF-H)) 11: VLD (Valid 8b/10b Symbol state with DIF-L or (DIF-H))
TD	Width 8 or 16	Input	Transmit Data for Tx Block
TDM	Width 1 or 2	Input	TD Coding Mode (0: D-Symbol, 1: K-Symbol) LP
TDR*	Width 8 or 16	Input	Transmit Data for Rx Block
TDRM*	Width 1 or 2	Input	TDR Coding Mode (0: D-Symbol, 1: K-Symbol)
MODE	Width 1	Input	PHY Power Mode (0: Dormant state, 1: After exiting from Dormant)

Note: [*] Indicates that these signals are used only for Half-duplex mode of operation.

3.1 Deliverables

- GDSII database
- LVS Netlist
- Physical Abstract Model (LEF)
- Timing Models

- Behavioral Models
- Design Integration Guide
- Technical Documentation

3.2 Related Products

- SD4.1 Device IP
- SD4/SDIO4/eMMC4.5 Host IP
- SD4/SDIO4/eMMC4.5 Hardware Validation Platform