Arasan
The Bus Stops Here

PRODUCT OVERVIEW

USB 1.1 Host IP Core

Features

- USB 1.1 compliant
- Supports 12 Mbit/s (FS) and 1.5 Mbit/s (LS) transfer rates
- Supports 127 devices
- Three downstream USB 1.1 ports
- Compliant to Open Host Controller Interface (OHCI)
- Supports asynchronous communication between CPU host and USB devices
- 48 MHz system clock
- 32-bytes PCI FIFO
- Two 32-byte ping-pong buffers for USB IN/OUT transfers
- Synthesizable VHDL/Verilog source code
- Optional 300 MHz 32-bit AHB or APB bus
- Optional 33 MHz PCI Rev. 2.2 bus
- Optional Custom bus for x86, SH3, 8051, ARM, ARC, and other processors
- Technology independent design
- Comprehensive test bench available

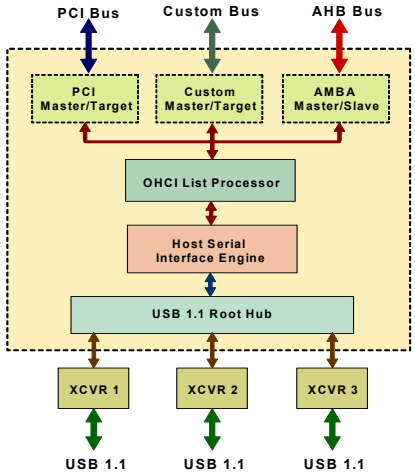
Overview

The Arasan USB 1.1 Host IP Core is an USB 1.1 compliant host core with an optional AHB, APB, PCI, or Custom bus interface. The USB 1.1 host core supports 12 Mbit/s in Full Speed (FS) mode and 1.5 Mbit/s in Low Speed (LS) mode.

The support on AHB, APB, PCI and Custom buses provides a direct interface to a wide variety of processors such as the ARM, x86, 8051, SH3, and ARC.The Arasan USB 1.1 Host IP Core implements the USB 1.1 host controller that compliant to the OHCI 1.0 specification.The USB host controller consists of the CPU host interface, OHCI List Processor, Host Serial Interface Engine, and USB 1.1 Root Hub. The Root Hub supports three downstream ports and is expandable as required. Up to a maximum of 127 devices can be supported by the USB host controller. The USB 1.1 Device IP Core consists of a 32-bytes PCI FIFO, and two 32-bytes ping-pong buffers for handling USB IN/OUT transfers.

The Arasan USB 1.1 Device IP Core is an RTL design in that implements an USB device controller on an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications. The IP core is silicon proven and in production with multiple customers.

USB 1.1 Host IP Core Functional Block Diagram



USB 1.1 Host IP Core

OHCI List Processor:

The OHCI List Processor manages data flow between the SIE and host processor. It also responsible for scheduling and executing of I/O Request Packets (IRPs) forwarded from the USB driver. The OHCI List Processor creates and manages Endpoint Descriptors (EDs) and Transfer Descriptors (TDs) that are located in the Host Controller Communication Area (HCCA).

USB 1.1 Root Hub:

The Root Hub consists of the USB 1.1 hub repeater. It handles functions such as the connectivity setup and tear down, babble detection and recovery, loss of activity, detection of connection and disconnection. Up to three USB 1.1 transceivers can be connected to the Root Hub and the number of port supported is expandable.

Serial Interface Engine:

Outgoing USB framed data from the device controller is serialized by the SIE. Serialized output data from the SIE is handled by a standard external USB transceiver such as the one provided by Philips. Incoming USB data from the transceiver is deserialized by the SIE. Other functions performed by the SIE include CRC generation/checking, and NRZI encoding/decoding.

AHB/APB Bus Interface:

Optional AHB or APB bus can be used to provide a high-speed interface for the USB 1.1 Device IP Core. The AHB/APB master is responsible for transferring data between the ARM Processor and USB 1.1 Device IP core. The AHB/APB slave Block consists of the Operational registers. Reading and writing of these registers are handled by the USB Device IP Core-AHB/APB bridge or ARM Processor.

PCI Bus Interface:

PCI Target/Master can be implemented that conforms to PCI specifications 2.2. The PCI Target/Master includes the DMA controller, configuration registers, PCI Power Management logic, and interrupt controller.

Custom Bus Interface:

Optional modules including general purpose buses such as the 8-bit parallel bus, 16-bit parallel bus, I2C bus, and SPI buses. The wide variety of custom buses supported enable the selection of different types of processors such as the x86, SH3, 8051, ARC and other processors. Custom buses with special requirements can also be implemented.

Benefits

- Complete hardware and software solutions
- Fully compliant USB 1.1 Host IP Core
- Premier direct support from Arasan IP core designers

Deliverables

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Item:

- Hardware evaluation kit available

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Data Sheet Links:

USB 1.1 IP Cores:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com