Arasan
The Bus Stops Here

PRODUCT OVERVIEW

USB 1.1 Device IP Core

Features

- USB 1.1 compliant
- Supports 12 Mbit/s (FS) and 1.5 Mbit/s (LS) transfer rate
- Supports all USB standard requests
- Supports class specific commands
- Ping-pong buffer for each isochronous endpoint
- Optional ROM for control endpoint configurations
- Expandable number of bulk, interrupt, control, and isochronous endpoints
- Digital phase lock loop recovery scheme
- Optional 300 MHz 32-bit AHB or APB bus
- Optional 33 MHz PCI Rev. 2.2 bus
- Optional Custom bus for x86, SH3, 8051, ARM, ARC, and other processors
- Technology independent design
- Comprehensive test bench available

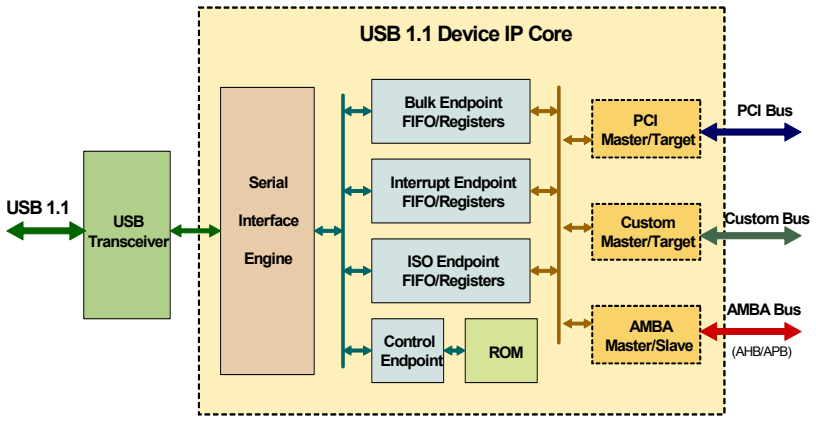
Overview

The Arasan USB 1.1 Device IP Core is an USB 1.1 compliant device core with optional AHB, APB, PCI, or Custom bus interface. The USB 1.1 device core supports 12 Mbit/s in Full Speed (FS) mode and 1.5 Mbit/s in Low Speed (LS) mode.

The USB 1.1 Device IP Core is highly configurable. The control endpoints and Serial Interface Engine (SIE) comprise of the basic building block of an USB 1.1 application. A design can be customized by adding the required number of bulk, interrupt, control, and isochronous endpoints. The control endpoint responsible for the configuration of the USB device, controlling of certain aspects of the device's operation, issuing of commands, reading of descriptors, and assignment of unique address to a device. A ROM can be included to hold the operational and control data for the control endpoints. Each isochronous endpoint comes with a ping-pong buffer suitable for isochronous data transfers.

The Arasan USB 1.1 Device IP Core is an RTL design in Verilog that implements an USB device controller on an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications. The IP core is silicon proven and in production with multiple customers.

USB 1.1 Device IP Core Functional Block Diagram



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USB 1.1 Device IP Core

Serial Interface Engine:

Outgoing USB framed data from the device controller is serialized by the SIE. Serialized output data from the SIE is handled by a standard external USB transceiver such as the one from Philips or other vendors. Incoming USB data from the transceiver is deserialized by the SIE.

Device Endpoints:

The number of bulk, interrupt, isochronous, and control endpoints can be customized to meet the design requirements. FIFOs associated with the endpoints can also be customerized. Dedicated ROM can be added to configure the USB device during power-up.

Device Controller:

The embedded USB 1.1 device controller responsible for the assemble and disassemble of USB frames. Operations of the bulk, interrupt, control, and isochronous endpoints are controlled by the device controller. Other functions of the device controller includes the issuing of commands, and controlling of bulk, interrupt, control, and isochronous transfers.

AHB/APB Bus Interface:

Optional AHB or APB bus can be used to provide a high-speed interface for the USB 1.1 Device IP Core. This AHB/APB master is responsible for transferring data between the ARM Processor and USB 1.1 Device IP core. The AHB/APB slave Block consists of the Operational registers. Reading and writing of these registers are handled by the USB Device IP Core-AHB/APB bridge or Arm Processor.

PCI Bus Interface:

PCI Target/Master can be implemented that conforms to PCI specifications 2.2. The PCI Target/Master includes the DMA controller, configuration registers, PCI Power Management logic, and interrupt controller.

Custom Bus Interface:

Optional modules including general purpose buses such as the 8-bit parallel bus, 16-bit parallel bus, I2C bus, and SPI buses. The wide variety of custom buses supported enable the selection of different types of processors such as the x86, SH3, 8051, ARC and other processors. Custom buses with special requirements can also be implemented.

Benefits

- Complete hardware and software solutions
- Fully compliant USB 1.1 Device IP Core
- Premier direct support from Arasan IP core designers
- Hardware Evaluation Kit available
- Client drivers and source code

Deliverables

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Item:

- Evaluation board available

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Data Sheet Links:

USB 1.1 IP Core:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com