DATASHEET

MIPI M-PHY Type 1

LLI Compatible

Arasan Chip Systems, Inc
2010 North First Street, Suite #510
San Jose, CA 95131
Ph:408-282-1600
Fx:408-282-7800
www.arasan.com

February, 2012

DISCLAIMER

This document is written in good faith with the intent to assist the readers in the use of the product. Circuit diagrams and other information relating to Arasan Chip Systems' products are included as a means of illustrating typical applications. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. Information contained in this document is subject to continuous improvements and developments.

Arasan Chip Systems' products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of Arasan Chip Systems Inc. will be fully at the risk of the customer.
Arasan Chip Systems Inc. disclaims and excludes any and all warranties, including without limitation any and all implied warranties of merchantability, fitness for a particular purpose, title, and infringement and the like, and any and all warranties arising from any course or dealing or usage of trade.

This document may not be copied, reproduced, or transmitted to others in any manner. Nor may any use of information in this document be made, except for the specific purposes for which it is transmitted to the recipient, without the prior written consent of Arasan Chip Systems, Inc. This specification is subject to change at anytime without notice. Arasan Chip Systems Inc. is not responsible for any errors contained herein.

In no event shall Arasan Chip Systems Inc. be liable for any direct, indirect, incidental, special, punitive, or consequential damages; or for lost of data, profits, savings or revenues of any kind; regardless of the form of action, whether based on contract; tort; negligence of Arasan Chip Systems or others; strict liability; breach of warranty; or otherwise; whether or not any remedy of buyers is held to have failed of its essential purpose, and whether or not Arasan Chip Systems Inc. has been advised of the possibility of such damages.

Restricted Rights
Use, duplication, or disclosure by the Government is subject to restrictions as set forth in FAR52.227-14 and DFAR252.227-7013 et seq. or its successor.

Copyright Notice
No part of this specification may be reproduced in any form or means, without the prior written consent of Arasan Chip Systems, Inc.

Questions or comments may be directed to:
Arasan Chip Systems Inc
2010 North First Street
Suite 510, San Jose, CA 95131.
Ph: 408-282-1600
Fx: 408-282-7800
Email: sales@arasan.com
http://www.arasan.com

CONTENTS

1 INTRODUCTION

1.1 Overview of MIPI M-PHY Devices

The M-PHY is a low pin count, power efficient, inter-chip serial interface with high bandwidth capabilities. An M-PHY configuration (LINK) consists of a minimum of two unidirectional lanes along with associated lane management logic.

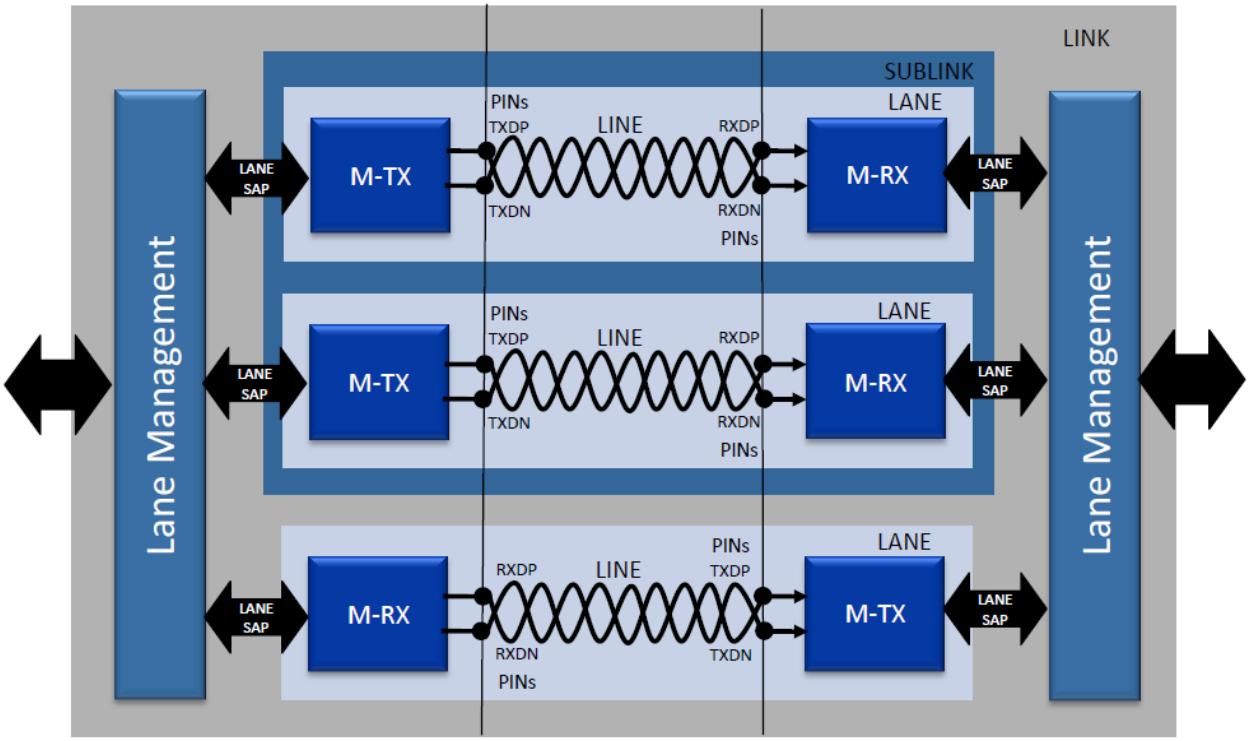

Figure 1: Example of MIPI M-PHY Link

1.1.1 Lanes

Each of the M-PHY lanes consists of a lane module (M-TX) that communicates to a corresponding module (M-RX) on the other chip via a serial interconnect that consists of two differential lines. The I/O functions of each lane module are managed by Lane Control and Interface Logic blocks.

1.1.2 Signalling

The differential lines can carry both High-Speed (HS) and Low-Speed (LS) signals, which have either a low voltage swing of 100 mV (Small Amplitude) or 200mV (Large amplitude). High-Speed functions are used for High-Speed Data traffic. The Low-Speed functions are mainly used for control and can have data transfer support.

1.1.3 Line Coding

All data transmitted (high-speed and low-speed) are 8b10b encoded. The target Bit Error Rate (BER) for any MPHY based PHY link is 10^{-10}.

1.1.4 M-PHY Type

In general, M-PHY can be either of Type-I or Type-II. Both systems have similar functionality and features for the High-Speed mode with support for HS-Gear1, HS-Gear2 and/or HS-Gear3. They however do differ in terms of Low-Speed functionality. Figure below summarizes the available speeds between Type-I and Type-II systems.

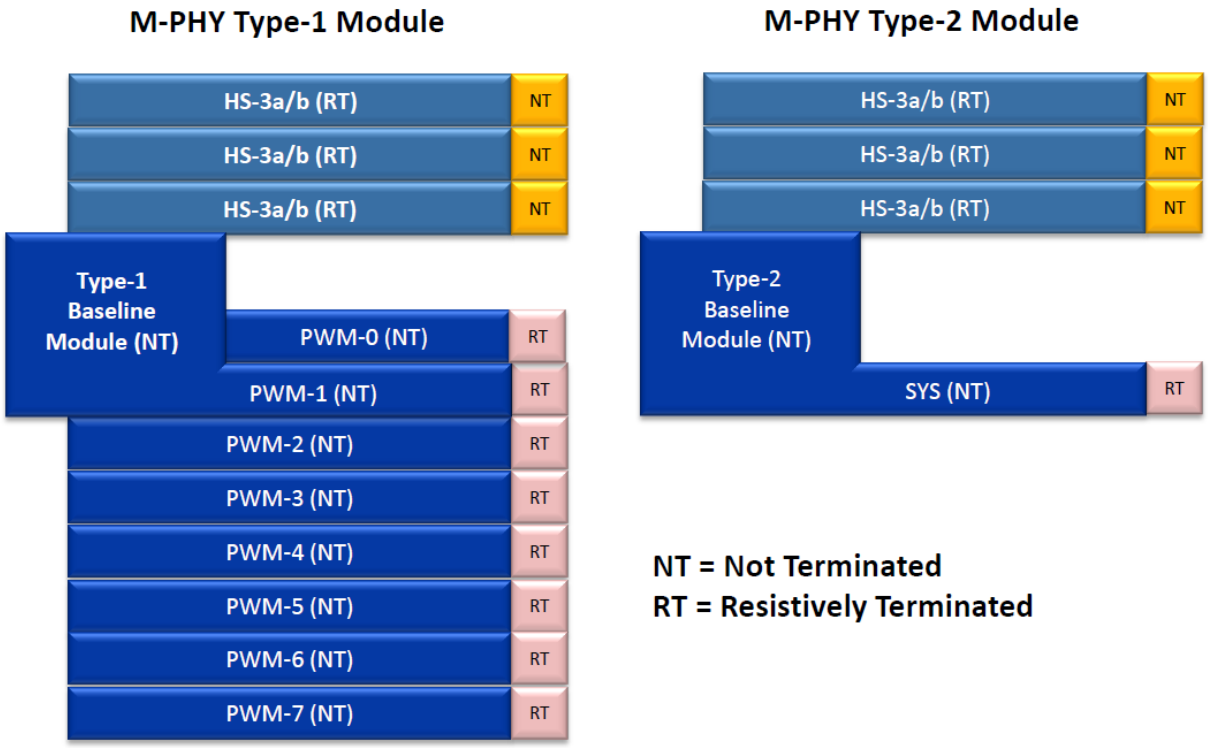

Figure 2: Types of M-PHY

1.2 Overview of Arasan M-PHY for LLI

Arasan's M-PHY fulfills the LLI requirements for M-PHY and implements an area and power efficient solution targeted for LLI. The M-PHY consists of analog transceivers, high speed PLL, data recovery units as well as the state-machine control all in a single GDSII. The interface to the LLI controller is compliant to M-PHY PIF specification, which allows seamless integration of the two IPs into the chip design.

2 FEATURES

- Compliant to MIPI Alliance Standard for M-PHY specification Version 2.0
- Supports high speed data transfer G1A/B and G2A/B with data rates of up to 2915.2 Mbps
- Supports M-PHY Type-I system
- Support for reference clock frequencies of 19.2MHz/26MHz/38.4MHz/52MHz
- Support for Clock and Data Recovery Options, as defined in LLI specification
    - Reference clock shared between transmitter and receiver to implement a mesochronous link
    - Independent reference clocks for transmitter and receiver to support a plesiochronous link
- Supports low speed transfer G0-G7 with a bit rate of up to 576 Mbps
- PWM signalling for Low speed [LS] data
- Supports error detection mechanism for sequence errors and contentions
- Data lanes support transfer of data in high speed mode
- Supports LS burst, HS burst, STALL, SLEEP, HIBERN8 states
- Supports squelch detection
- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PIF (RMMI)
- Activates and disconnects high speed terminators for reception and transmission
- Supports standard PHY transceiver compliant to MIPI Specification
- Supports standard PIF (RMMI) interface compliant to MIPI Specification.
- On-chip clock generation configurable for either transmitter or a receiver
- Testability for Tx, Rx and PLL

3 ARCHITECTURE

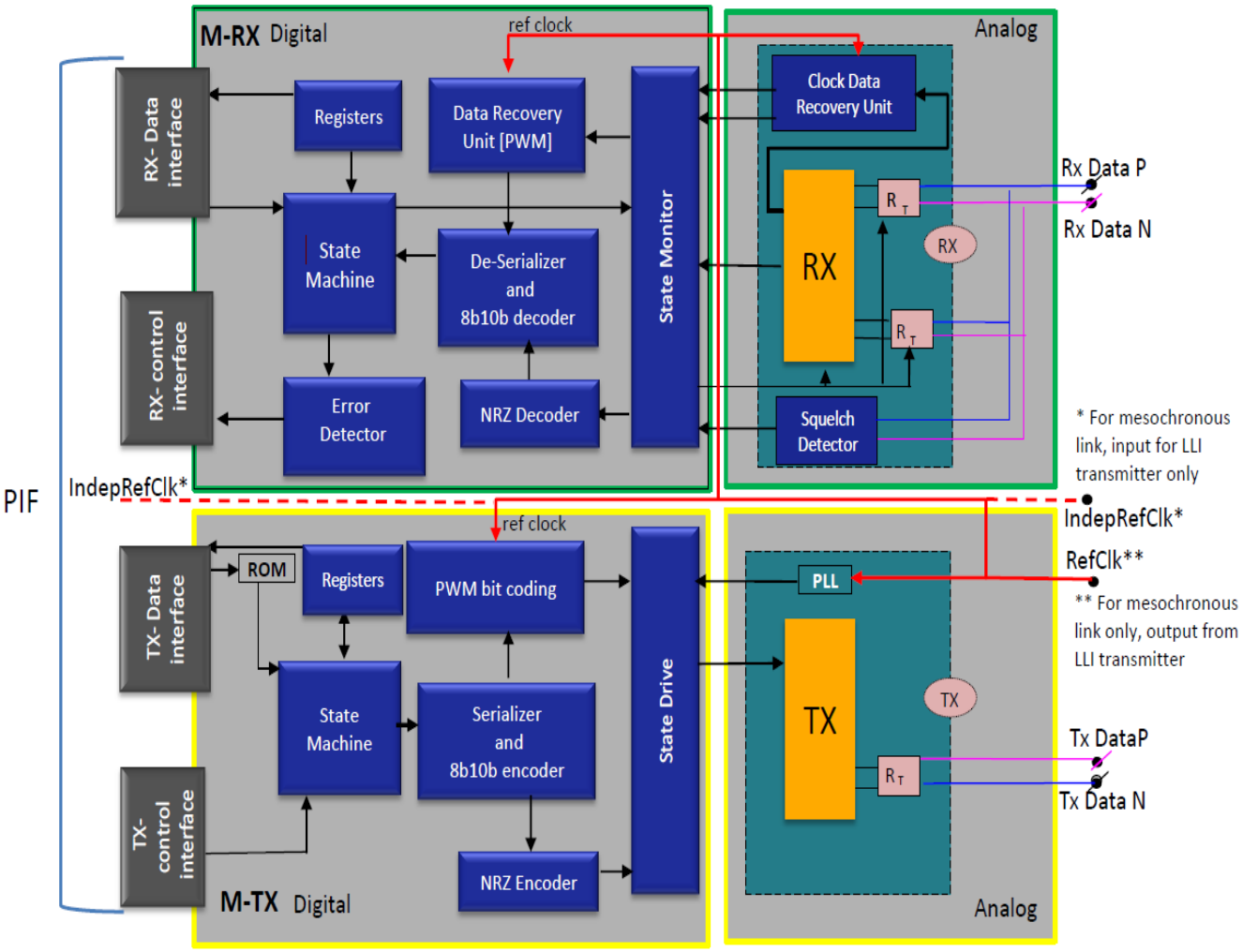

Figure 3: M-PHY Sub-Link Functional Block Diagram

4 M-PHY PAD TABLE

Table 1: M-PHY Pads for each Tx Lane

Pins	Direction	Description
TxDataP	OUTPUT	Positive polarity of low voltage differential clock signal for transmitter
TxDataN	OUTPUT	Negative polarity of low voltage differential clock signal for transmitter

Table 2 : M-PHY Pads for each Rx Lane

Pins	Direction	Description
RxDataP	INPUT	Positive polarity of low voltage differential data signal for receiver
RxDataN	INPUT	Negative polarity of low voltage differential data signal for receiver

Table 3: Reference Clock

Pins	Direction	Description
RefClk	INPUT (LLI Rx)/OUTPUT (LLI Tx)	Shared reference clock for mesochronous links only
IndepRefClk	INPUT	Independent reference clock for LLI transmitter and receiver for plesiochronous links only

Table 4: Protocol Interface (PIF) Signals - M-TX-CTRL Interface Signals

Signal Name	Direction	Description
TX_CfgClk	INPUT	Transmit Control Interface Clock
TX_Reset	INPUT	Active-high asynchronous reset to reset M-TX. Should be asserted for at least 100 ns
TX_AttrID[7:0]	INPUT	This signal indicates the configuration attributes for read or write operations, or M-TX Capability attribute or OMCS Status Attributes for read operation
TX_AttrRdVal[7:0]	OUTPUT	Attribute Read data from M-TX
TX_AttrWrVal[7:0]	INPUT	Attribute Write data to M-TX
TX_AttrWrn	INPUT	Attribute write enable to M-TX. ‘1‘ - Write operation. ‘0’ - Read operation.
TX_CfgEnbl	INPUT	Configuration Enable to M-TX. This signal indicates an enable for attribute read or write operation.

Signal Name	Direction	Description
TX_InLnCfg	INPUT	TX_InLnCfg is used in conjunction with TX_AttrWrn and TX_CfgEnbl to direct an write operation to the M-TX's shadow memory bank or to the M-TX's effective configuration bank. '0' - shadow memory bank. '1' - effective configuration Note: UniPro can only read from the effective configuration bank.
TX_CfgUpdt	INPUT	This signal indicates to transfer the contents of the shadow memory to the effective configuration bank.
TX_CfgRdyN	Output	This signal indicates whether M-TX is ready to accept write data. '0' - M-TX is ready to accept write data. '1' - M-TX is not ready to accept write data.
TX_LineReset	INPUT	This signal indicates M-TX to issue LINERESET.
TST_RTControl	INPUT	TST_RTControl carries real-time signals to control implementation-specific signals, e.g. test features, inside the M-TX. These signals are asynchronous to any clock on the M-TXDATA or M-TX-CTRL interfaces.

Table 5: Protocol Interface (PIF) Signals - M-TX Data Interface Signals

Signal Name	Direction	Description
TX_SaveState_Status_N	OUTPUT	TX_SaveState_Status_N indicates the MTX is entering or exiting a SAVE state. The Protocol Layer can use this signal to understand when the M-TX is not transmitting PREPARE, SYNC, HOB, PAYLOAD, TOB, BURST Extension or LINE-CFG information. The M-TX sets tx_savestate_status_n to "0" when it enters into a SAVE state. The M-TX sets tx_savestate_status_n to "1" when it exits a SAVE state.
TX_SymbolClk	INPUT	M-TX DATA Symbol Clock
TX_PhyDIRDY	OUTPUT	PHY Data Input Ready. This signal indicates that M-TX is ready to accept new data.
TX_Symbol[39:0]/[19:0]/[9:0]	INPUT	TX_Symbol is used for BURST data transfer to the M-TX. The contents of this bus depend on the whether the 8b10b encoding function in the M-TX is bypassed. When the M-TX 8b10b encoding function is bypassed, TX_Symbol carries the raw data to send on the LINEs, parallelized according to the implemented width. The LSb of TX_Symbol shall correspond to the earliest transmitted bit. When the M-TX 8b10b encoding function is enabled, 16 LSbs of TX_Symbol are used to carry the unencoded DATA or control symbol. The M-TX shall ignore the unused MSbs of TX_Symbol.
TX_ProtDORDY[3:0]/[1:0]/[0]	INPUT	PHY Data Output Ready This signal indicates that data is available in the corresponding tx_symbol.

Signal Name	Direction	Description
TX_DataNCtrl[3:0]/[1:0]/[0]	INPUT	TX_DataNCtrl indicates the type of symbol on TX_Symbol. The bits of TX_DataNCtrl are mapped to the same as the bits of TX_ProtDORDY. '0' - data symbol. '1' - control symbol.
TX_Burst	INPUT	This active high signal indicates that burst is in progress.
TST_RTObserve	OUTPUT	TST_RTObserve makes internal M-TX real time signals observable, e.g. through DMA, by the Protocol Layer, or external test equipment. These signals are asynchronous to any clock on the M-TX-DATA or M-TX-CTRL interfaces.

Table 6: Protocol Interface (PIF) Signals - M-RX CTRL Interface Signals

Signal Name	Direction	Description
RX_CfgClk	INPUT	Receive Control Interface Clock.
RX_Reset	INPUT	Active-high asynchronous reset to reset M-RX. Should be asserted for at least 100 ns.
RX_LineReset	OUTPUT	This signal indicates the status of LINERESET. '1' - LINERESET is detected. '0' - LINERESET is in exit state
RX_AttrID[7:0]	INPUT	This signal indicates the configuration attributes for read or write operations, or M-RX Capability attribute or OMCS Status Attributes for read operation.
RX_AttrRdVal[7:0]	OUTPUT	Attribute read value from M-RX.
RX_AttrWrVal[7:0]	INPUT	Attribute write value to M-RX.
RX_AttrWrn	INPUT	Attribute write enable to M-RX. '1' - Write operation. '0' - Read operation.
RX_CfgEnbl	INPUT	Configuration Enable to M-RX. This signal indicates an enable for attribute read or write operation.
RX_InLnCfg	INPUT	RX_InLnCfg is used in conjunction with RX_AttrWrn and RX_CfgEnbl to direct a write operation to the M-RX's shadow memory bank or to the M-RX's effective configuration bank. '0' - shadow memory bank. '1' - effective configuration Note: UniPro can only read from the effective configuration bank.
RX_CfgUpdt	INPUT	RX_CfgUpdt transfers the contents of the INLINE-CR registry to the effective configuration bank during a SAVE state..
RX_CfgRdyN	OUTPUT	This signal indicates whether M-RX is ready to accept write data. '0' - M-RX is ready to accept write data. '1' - M-RX is not ready to accept write data.

Signal Name	Direction	Description
RX_Hibern8Exit_Type-I	OUTPUT	RX_Hibern8Exit_Type-I indicates the M-RX is exiting HIBERN8. The M-RX sets RX_Hibern8Exit_Type-I to "1" when it detects a DIF-Z to DIF-N transition on the LINE. The M-RX sets RX_Hibern8Exit_Type-I to "0" when the MRX is in either HIBERN8 or DISABLED state.
RX_LCCRdDet	OUTPUT	RX_LCCRdDet indicates that M-RX received an LCC-READ sequence, which results in the update of corresponding attributes in the M-RX.
TST_RTControl	INPUT	TST_RTControl carries real-time signals to control implementation-specific signals, e.g. test features, inside the M-RX. These signals are asynchronous to any clock on the M-RXDATA or M-RX-CTRL interfaces.

Table 7: Protocol Interface (PIF) Signals - M-RX Data Interface Signals

Signal Name	Direction	Description
RX_SymbolClk	INPUT	M-RX DATA Symbol Clock
RX_Symbol[39:0]/[19:0]/[9:0]	INPUT	RX_Symbol is used for BURST data transfer from the M-RX. When the 10b8b decoding function is bypassed, RX_Symbol carries the raw data as received on the LINEs, parallelized according to the implemented width. The LSb of RX_Symbol shall correspond to the earliest received bit. When the 10b8b decoding function is enabled, only the 16 LSbs of RX_Symbol are used to carry the decoded DATA or control symbol. The MRX shall set the remaining MSbs to "0".
RX_PhyDORDY[3:0]/[1:0]/[0]	INPUT	PHY Data Output Ready This signal indicates that data is available in the corresponding RX_Symbol.
RX_DataNCtrl[3:0]/[1:0]/[0]	INPUT	TX_DataNCtrl indicates the type of symbol on RX_Symbol. The bits of RX_DataNCtrl are mapped to the same as the bits of RX_ProtDORDY. '0' - data symbol. '1' - control symbol.
RX_SymbolErr[3:0]/[1:0]/[0]	INPUT	This signal is asserted when anyone of the following error • The 3b4b sub-block is in error while decoding the related 8b10b symbol received over the LINE • The 5b6b sub-block is in error while decoding the related 8b10b symbol received over the LINE • The Running Digital Sum algorithm computes an RDS error for the related 8b10b symbol received over the LINE • The related 8b10b symbol received over the LINE is a reserved symbol The M-RX shall set all bits of RX_SymbolErr to "0" for all other conditions.
RX_Burst	INPUT	This active high signal indicates that burst is in progress.

Signal Name	Direction	Description
TST_RTObserve	OUTPUT	TST_RTObserve makes internal M-RX real time signals observable, e.g. through DMA, by the Protocol Layer, or external test equipment. These signals are asynchronous to any clock on the M-RX-DATA or M-RX-CTRL interfaces.

Table 8: Power Pads

Pins	Types	Direction	Description
VDD	POWER	INOUT	Power supply for Lanes
VSS	POWER	INOUT	
VDDD	POWER	INOUT	Power supply for Digital M-PHY
VSSD	POWER	INOUT	
VDDPLL	POWER	INOUT	Power supply for PLL
VSSPLL	POWER	INOUT	
VDDB	POWER	INOUT	Power supply for Bias Generation
VSSB	POWER	INOUT	

Table 9: Analog Configuration bit (trim bits)

Number	Register	Direction	Description
1	trim_0[31:0]	INPUT	Trim bits for M-PHY
2	trim_1[31:0]	INPUT	Trim bits for M-PHY
3	trim_2[31:0]	INPUT	Trim bits for M-PHY
4	trim_3[31:0]	INPUT	Trim bits for M-PHY

5 Hard Macro Deliverables

The full IP package complete with:

- User Guide and Integration Guides
- GDS-II
- CDL Netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- LEF
- Scan-inserted Netlist for DFT
- Verification Environment with behavioral models

