DATASHEET

I2S Controller

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1 INTRODUCTION

The Arasan I2S Controller IP Core is a two-channel I2S serial audio controller compliant to the Philips* Inter-IC Sound specification. The I2S bus is used for connecting audio components such as speakers, DACs, or audio subsystems.

The Arasan I2S Controller can simultaneously send and receive data through the I2S bus. This simultaneous operation is provided by the presence of two separate FIFOs for transmission and reception. The transmit FIFO and receive FIFO handle data transfers between the I2S interface and application interface. These two interfaces can be operated in two independent clock domains. The I2S Controller also includes interrupt support for reporting FIFO and other conditions. The I2S transmitter and receiver can be configured for both I2S master and I2S slave modes through the configuration registers. The IP supports two channels with 32-bit audio resolution by default. The DAC/ ADC resolution can be configured as 8/16/24/32 bit wide.

1.1 Overview

The Arasan I2S Controller IP Core provides a 32-bit parallel processor bus as the application interface. The controller's I2S interface consists of one transmitter and one receiver. Each channel can be programmed as an I2S master or an I2S slave. The Bit Clock (BLCK) and Left and Right Clock (LRCK) provide synchronization to transmit and receive data. The I2S Controller IP supports 44.1KHz audio sampling rates. DAC/ADC resolution is configurable from 8-bit to 32-bit. The I2S Controller IP supports a 32-bit parallel bus interface. AHB, PCI or other custom specific buses can also be provided upon request.

1.2 Features

- Complies with Philips* I2S Specification
- Supports two I2S channels
- Simultaneous audio playback and recording
- Supports configurable 8/16/24/32 bit DAC/ADC resolution
- Supports 44.1KHz audio sampling frequencies
- 32-bit parallel processor bus
- Interrupt support for FIFO transfers
- Supports 256 sampling frequency operating modes
- Other custom buses available upon request

2 ARCHITECTURE

The principle components of the Arasan Parallel I2S Controller are Parallel Bus Interface, Transmit FIFO, Receive FIFO, I2S Controller, Transmitter, and Receiver. The below figure depicts the block diagram of the I2S Controller.

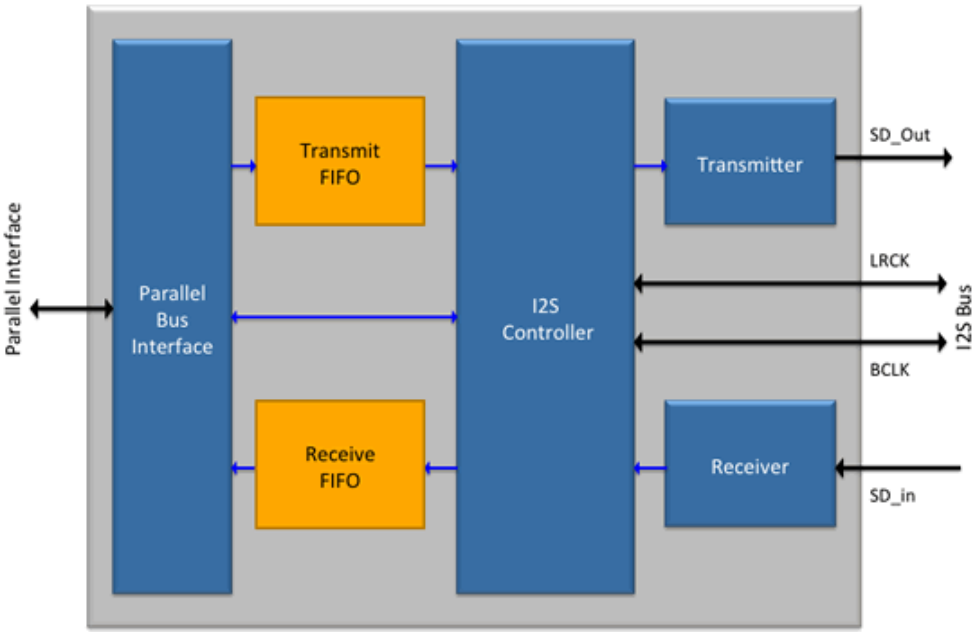

Figure 1: I2S Controller Core IP Block Diagram

2.1 Parallel Bus Interface

The Arasan I2S controller uses a parallel interface to connect to any processor's parallel bus. The I2S Controller provides a 32-bit parallel processor bus interface. It consists of various control and status registers. The processor can access these registers through the parallel bus that provides two 32-bit wide data buses for simultaneous read and write operations. The I2S transmitter and receiver can be enabled or disabled through the enable registers in this block. The transmit ready (FIFO empty) and receive data ready (FIFO full) interrupts can also be enabled or disabled. The transmission or reception of data can be programmed through the data port register.

2.2 I2S Controller

The I2S Controller controls the operation of the I2S transmitter and receiver. It directs data from the transmit FIFO to the transmitter and from the receiver to the receive FIFO. It also generates the bit clock (BCLK) and left-right clock (LRCK). These clocks are generated from a crystal oscillator source.

2.3 Transmit FIFO

The transmit FIFO and receive FIFO provide a means of data buffering. It stores data from the source until it is read by the sink. The FIFO's depth can be parameterized. To the transmit FIFO, the parallel bus is the source and transmitter is the sink. The receive FIFO stores data from the receiver until it is read by the parallel bus.

2.4 Receive FIFO

The I2S receiver stores data from SD_in input into the receive FIFO. It converts serial data from the SD_in input to parallel format and then stores it into the receive FIFO.

2.5 Transmitter

The I2S transmitter reads the 32-bit wide data from the transmit FIFO through the I2S controller. It shifts data serially out the SD_out line. Data shifting out the SD_out line is aligned to the LRCK clock output.
The transmitter interface can be programmed to operate as an I2S master or an I2S slave. There are two operating modes.

- Master Transmitter Mode - serial data is transmitted through SD_out while BCLK and LRCK are serial and word select clocks outputs respectively.
- Slave Transmitter Mode - serial data is transmitted via SD_out while BCLK and LRCK are serial and word select clocks inputs respectively.

2.6 Receiver

The receiver interface can be programmed to operate as an I2S master or an I2S slave. There are two operating modes.

- Master Receiver Mode - serial data is received via SD_in while BCLK and LRCK are serial and word select clocks outputs respectively.
- Slave Receiver Mode - serial data, serial clock and word select are received through SD_in, BCLK, and LRCK inputs respectively.

3 SIGNAL INTERFACES

The Arasan I2S Controller IP Core has a parallel interface and an I2S interface

Table 1: Parallel Interface

Pin Name	Direction	Description
sys_clk	Input	System Clock
rst_n	Input	Active Low System Reset
cs_n	Input	Active Low Chip Select
addr[2:0]	Input	System Address Bus
data_in[31:0]	Input	Parallel Data Input
data_out[31:0]	Output	Parallel Data Output
nRD_WR	Input	Read/Write 0: Read 1: Write

Table 2: I2S Interface

Pin Name	Direction	Description
clk_48	Input	48 MHz Crystal Oscillator Input
bclk	Output	Audio bit clock generated when I2S controller is in master mode
lrck	Output	Word Select generated when I2S controller is in master mode.
bclk_en	Output	Audio bit clock asserted when I2S controller is in master mode.
lrck_en OUT	Output	Word Select asserted when I2S controller is in master mode.
SD_out	Output	Serial Output
SD_in I	Input	Serial Input

4 SoC LEVEL INTEGRATION

4.1 Verification Environment

This section gives the detail about test environment of Arasan Parallel I2S Controller. Arasan PARALLEL I2S CONTROLLER has been verified in the simulation environment using the behavioral models of the surrounding environment (RTL Verification).

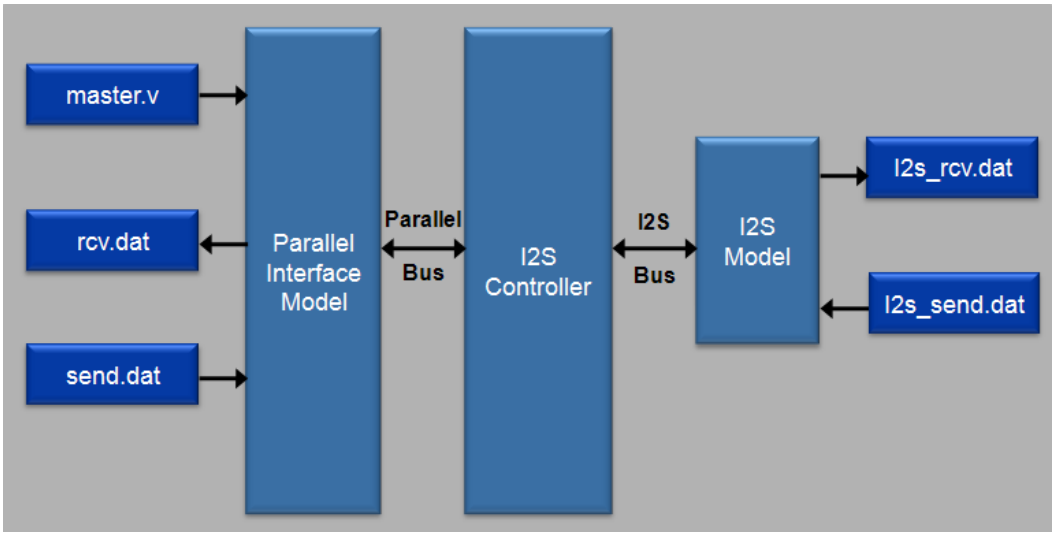

Figure 2: I2S Verification Environment

4.2 IP Deliverables

The IP package consists of the following:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

5 RELATED PRODUCTS

- I2C Controller
- SPI_AHB