USB1.1- AHB DEVICE CORE

(Technical Data Sheet)

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FEATURES

This section describes features of Arasan_Usb1.1_ahb_Device.

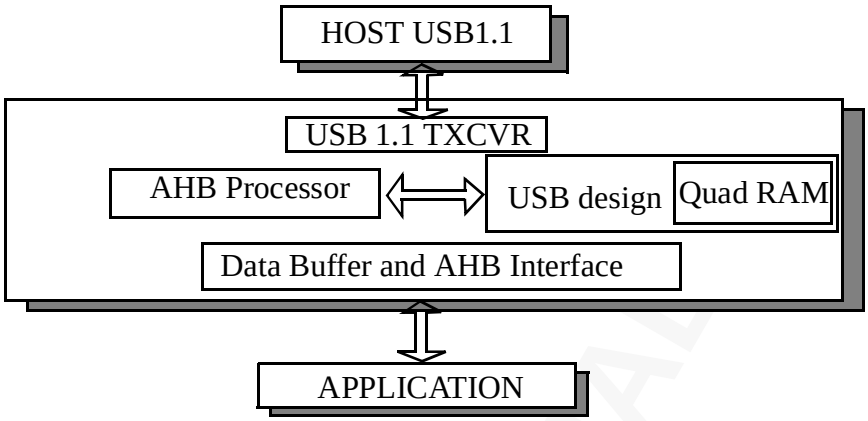
* Silicon proven
* VHDL/Verilog source code available.
* Soft Connect Feature
* FIFOs are housed inside the core for both data-out and data-in paths.
* Dramatically shortens design cycles.
* Optimized for the APEX 20K architectures.
* Supports control, interrupt, bulk and isochronous transfers.
* Application specific control transfer support.
* Multiple endpoints accessibility.
* AHB processor interface for programming the device
* AHB interface and HCI interface for data transfers.

GENERAL DESCRIPTOIN

In Prog_Arasan_usb1.1_device, the transceiver interfacing pins are compatible with Philips. The core operates at 12MHZ as well as at 1.5MHZ. The core has a generic processor interface and allows the local processor to configure the endpoints depending on the application and then declare a connection to the USB host.The device descriptor values are stored in the memory associated with the local processor.

FUNCTIONAL BLOCK DIAGRAM

The functional block diagram of Arasan_Usb1.1_ahb_Device is shown in Figure below



SIGNAL INTERFACE

USB design has 2 major interfaces namely Transceiver interface, Processor interface.

Transceiver interface PINS
Active low signals have been indicated with a suffix of '_n'.

PIN	Direction	Description
MODE	Out	When left unconnected, a weak pull-up transistor pulls it to VCC and in this mode. When connected to GND, the VMO/FSEO pin takes the function of FSEO (Force SEO).
OE#	Out	Output Enable. Active LOW, enables the transceiver to transmit data on the bus. When not active the transceiver is in receive mode
RCV	IN	Receive data. CMOS level output for USB differential input
VP, VM	IN	Gated version of D– and D+. Outputs are logic “0” and logic “1”. Used to detect single ended zero (SE0#), error conditions, and interconnect speed. (Inputs to SIE). VP VM RESULT 0 0 SE0# 0 1 Low Speed 1 0 Full Speed 1 1 Error

PIN	Direction	Description
SUSPND	Out	Suspend. Enables a low power state while the USB bus is inactive. While the suspnd pin is active it will drive the RCV pin to a logic “0” state. Both D+ and D– are tri-stated.
SPEED	Out	Edge rate control. Logic “1” operates at edge rates for “full speed”. Logic “0” operates edge rates for “low speed”.
VPO, VMO/ FSEO	Out	Inputs to differential driver. (Outputs from SIE). MODE VPO VMO/FSEO RESULT 0 0 0 Logic “0” 0 1 SE0# 1 0 Logic “1” 1 1 SEO# 1 0 0 SE0# 0 1 Logic “0” 1 0 Logic “1” 1 1 Illegal code

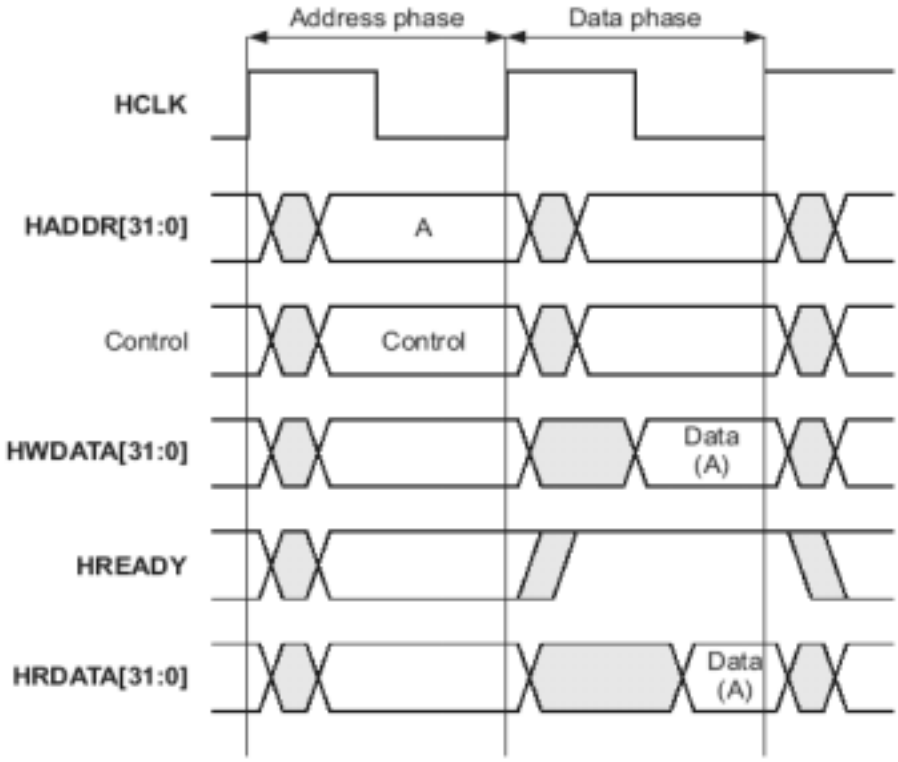
Processor Interface signals:

Pins	Direction	Description
HCLK	Input	This clk times all bus transfers.All signal timings are related to the rising edge of **HCLK**.
HRESETN	Input	The bus reset signal is active low and is used to reset the system and the bus.
HADDR1[31:0]	Input	The 32 bit system address bus.This signal is routed to the ahb target core.
HTRANS1[1:0]	Input	Indicates the type of the current transfer,which can be **nonsequential, sequential,idle** or **busy**.
HSIZE1[2:0]	Input	Indicates the size of the transfer,which is typically byte,halfword or word.
HBURST1[2:0]	Input	Indicates if the transfer forms part of a burst.Four,eight and sixteen beat bursts are supported and the burst may be either incrementing or wrapping.
HWDATA1[31:0]	Input	The write data bus is used to transfer data from the master to the bus slaves during write operations.

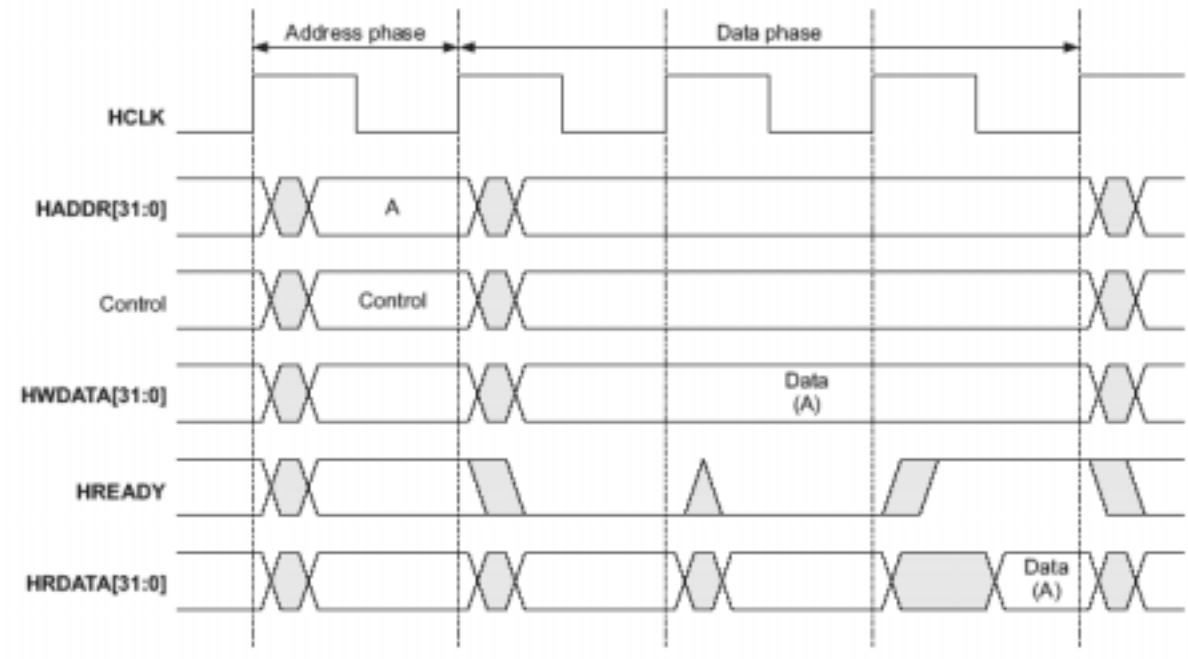
Pins	Direction	Description
HWRITE1	Input	When HIGH, this signal indicates a write transfer and when LOW a read transfer.
HRDATA1[31:0]	Output	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
HREADY1	Output	When HIGH ,this signal indicates that a transfer has finished on the bus.This signal is driven LOW to extend a transfer.This signal is routed to the master core.
HPROT1[3:0]	Input	The signal indicates if the transfer is an **opcode fetch** or **data access** or **user mode access**.For bus masters with a memory management unit these signals also indicate whether the current acess is cacheable or bufferable.
HRESP1[1:0]	Output	The transfer response provides additional information on the status of a transfer, **OKAY,ERROR,RETRY** or **SPLIT**.
HMASTER[3:0]	Input	This signal from the arbiter indicate which bus master is currently performing a transfer and is used by the slaves which support SPLIT transfers to determine which master is attempting an access.
INT	Output	An interrupt is generated each time the setup data registers or ata atapi cmd registers or status register is written by device.Interrupt is also generated when ep0_fb register's contents are transferred to the device.

DATA TRANSFER PROTOCOLS

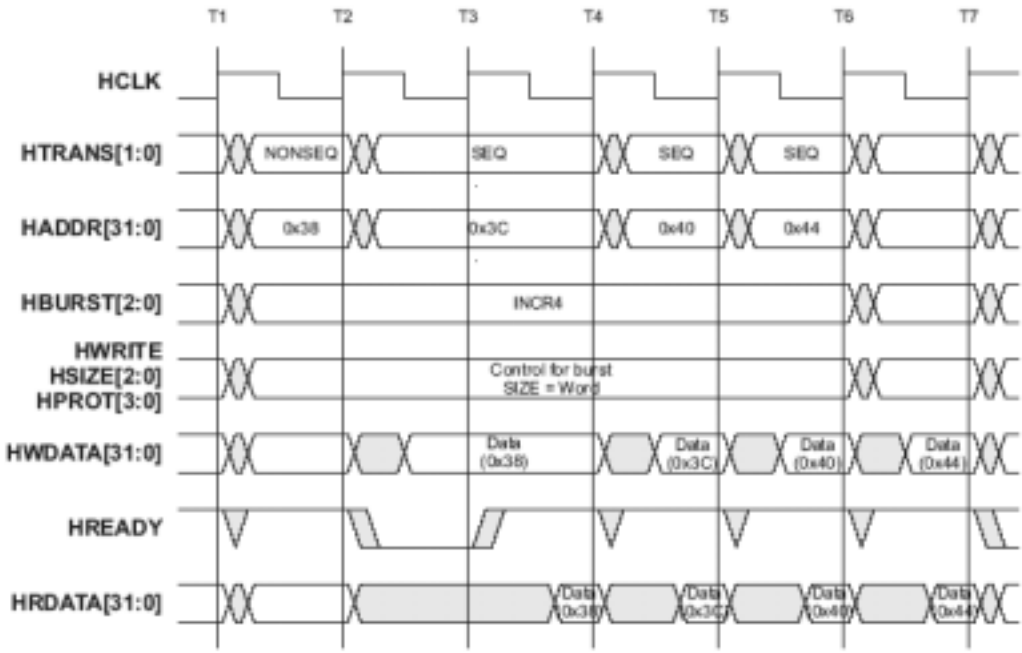
AHB SIMPLE DATA TRANSFER



AHB TRANSFER WITH WAIT STATES



AHB TRANSFER IN BURST MODE



PROGRAMMING INTERFACE

DEVICE CONTROLLER REGISTERS

Offset	Processor	Core	Description
00h	R/W	R	Control_reg
04h	R/W	R	Interrupt_enable_reg
08h	R/W	R	Interrupt_disable_reg
0ch	R/W	R/W	Interrupt_status_reg
10h	R	R/W	Setup_data_reg
18h	R /W	R	Ep0_feedback_reg
1ch	R/W	R	Ep1_characteristic_reg
20h	R/W	R	Ep2_characteristic_reg
24h	R/W	R	Ep3_characteristic_reg
28h	R/W	R	Ep4_characteristic_reg
2ch	R/W	R	Ep5_characteristic_reg
30h	R/W	R	Ep_feedback_reg
34h	R/W	R	Prog_polarity_reg
38h	R	R/W	Ep_status_reg
3ch	R/W	R	Address_reg
40h	R	R/W	Transmit_count_reg
44h	R/W	R/W	Receive_count_reg
48h	R/W	R	Hci_dma_acc_stat_reg
4ch	R/W	R	Ep0_in_data_reg
8ch	R	R/W	Ep0_out_data_reg
cch	R/W	R/W	Ep0_data_status_reg

PHYSICAL ESTIMATES

* Number of gates : 16k
* Quad Port Ram size: [1KB]

VERIFICATION

* IP modules are Silicon proven

DELIVERABLES

* RMM complaint VHDL or Verilog RTL
* Test bench with compliance & synthesis scripts
* Behavioural models
* Firmware source code in 'C' language
* FPGA evaluation board
* User manual
* On-site support for customization