Datasheet

MIPI CSI, DSI Physical Interface Total IP Solution

CPHY v1.2 Physical Interface
DPHY v1.2 Physical Interface

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1 Introduction

The ever increasing demand for band width for the high resolution cameras resulted in to search for a simple, cost effective, rate efficient PHY which can support above 2.5Gbps. This search resulted into a new kind of PHY, which even at less channel rate provides very high data rate.

CPHY1.2 can achieve a very high data rate of 6.84Gbps per lane compared to the 2.5Gbps of DPHY1.2 and its legacy, still maintain the channel rate at 3Gsps which is same as CPHY1.2. CPHY achieves this by using a unique encoding mechanism in which 16 bit of input data is encoded into 7 symbols and each symbol is transmitted over a 3 Phase encoded line.

With CPHY v1.2, the maximum channel rate achieved would be 3Gsps which would result in an effective data rate of 6.84Gbps.

CPHY reuses the similar Low power signaling same as the DPHY. CPHY is designed such a way that it can co-exist sharing the same lines as DPHY. CPHY/DPHY combo IPs will be compatible to operate on the same channels used by DPHY, which offer a much wider area of application and flexibility. It can work with both old DPHY systems and is compatible with new CPHY.

Arasan's ComPhy is a CPHY/DPHY combo universal PHY which can be configured both as Transmitter and Receiver. Arasan's novel and innovative design techniques allowed sharing a number of modules between the CPHY and DPHY with no impact on performance resulting in optimal area and power.

2 Features

- Compliant to DPHY 1.2 and CPHY 1.2
- Supports CSI 1.3
- Supports transfer at high speed mode with a bit rate of 182-6857Mbps for CPHY1.2
- Supports synchronous transfer at high speed mode with a bit rate of 40-2500Mbps for DPHY1.2
- Supports a channel rate of 3000Msps for CPHY
- CPHY/DPHY combo which can support both modes in same IP
- Supports asynchronous transfer at low power mode with a bit rate of 10 Mb/s
- Spaced one hot encoding for Low power [LP] data
- Supports Alternate Low Power(ALP) mode for CPHY 1.2
- Supports up to one clock lane and four data lanes for DPHY1.2
- Three 3phase encoded data lanes for CPHY1.2
- Clock recovery mechanism from the data streams for the CPHY
- Same physical lines are used for both CPHY and DPHY
- 16 bit to 7 symbol mapper and 3phase encoder for CPHY
- DPHY and CPHY shares same design elements providing optimal design footprint
- Deskew support for the DPHY 1.2
- Supports error detection mechanism for sequence errors and contentions
- Supports ultra-low power mode, high speed mode and control mode.
- Has clock divider unit to generate clock for parallel data reception and transmission from and to the PPI
- Activates and disconnects high speed terminators for reception and transmission.
- Supports standard PHY transceiver compliant to MIPI Specification
- Supports standard PPI interface compliant to MIPI Specification for both DPHY1.2 and CPHY1.2
- Clock lane supports unidirectional communication
- On-chip clock generation configurable for either transmitter or loopback (BIST)
- PHY can be configured as a master or slave.
- Testability for Tx, Rx and PLL
- Built in Self Test for CPHY and DPHY
- Core is structured to increase the number of data lanes.
- Supports scan insertion and stitching for DFT
- Supports additional flexibility in terms of data lane/line polarity swapping
- Provides extensive debug capability and access which facilitate easy silicon debug and device characterization

3 Architecture

3.1 C-PHY Based Interconnect Architecture

CPHY employs coding scheme in which clock can be recovered from the transmitted data. No separate clock lane is required in the interconnect and the slave will recover the clock from the data stream at the Slave side.

Each data lane is a 3 phase encoded requiring 3 separate line inter connections. Each lane interconnect provides up to 6.85 Gbps with effective data rate of 20.85 Gbps. Each data lane is a 3 phase encoded requiring 3 separate line inter connections. Each lane interconnect provides up to 6.85 Gbps with effective data rate of 20.85 Gbps.

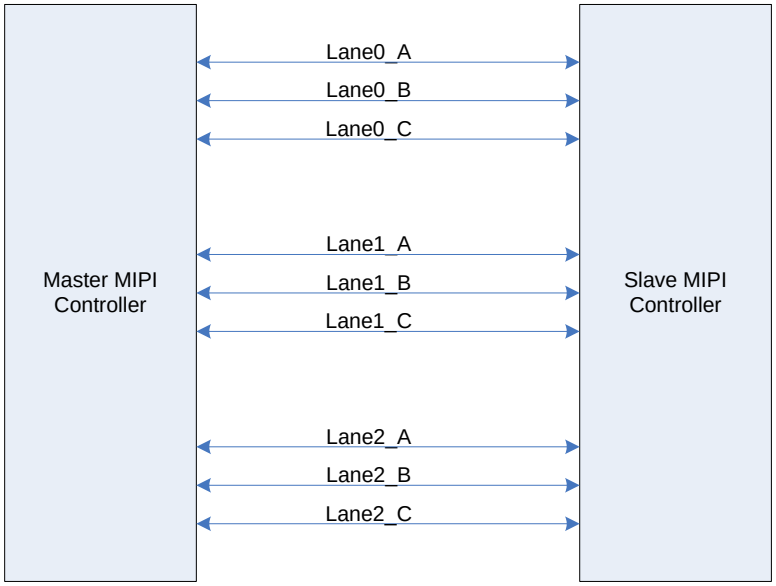

Figure 1: MIPI Link Diagram for CPHY

3.2 CPHY Lane Architecture

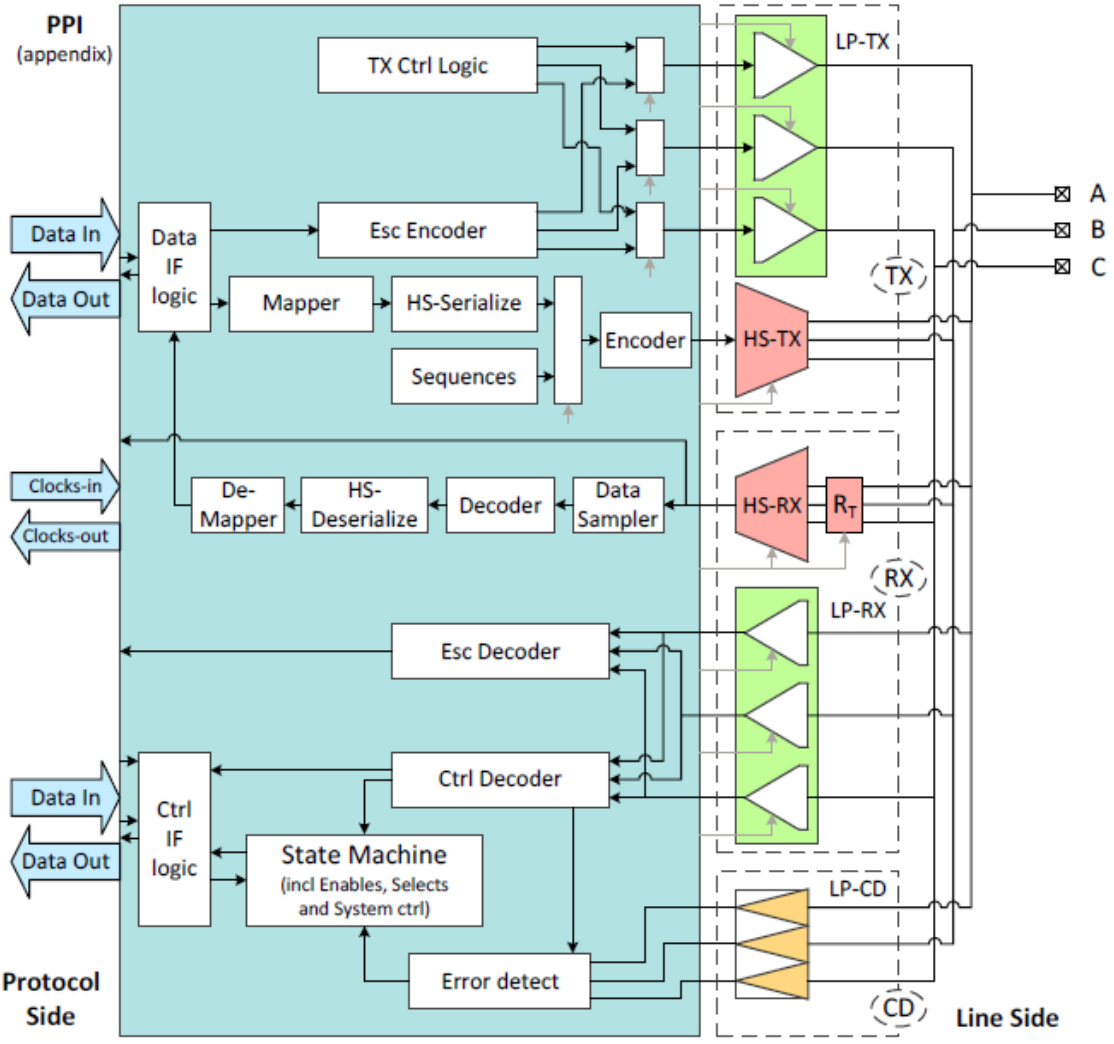

Figure 2: CPHY Lane Architecture

Each Lane Module has a control and interface logic unit and a transceiver portion to handle 3 Phase High-Speed functions, single-ended Low-Power functions operating on each of the interconnect wires individually. The I/O functions are controlled by a Lane Control and Interface Logic block.

High-Speed signals have a low voltage swing of 250 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

High Speed data width is 16bit at the PPI side, which is converted to 7 Symbols by the mapper. Each symbol is 3bit which is encoded into 3 phase signal by the encoder driver combination. Control and Interface Logic, sends and detects start of packet signaling and end of packet signaling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

3.3 D-PHY Based Interconnect Architecture

DPHY employs a source synchronous scheme in which the High speed clock is transmitted using a separate channel along with the data lane. The clock maintains quadrature phase relationship to the data lane to ensure maximum margin between the clock and the data lane. Each data lane consists of two wires (Dp/Dn) and data is transmitted as differential signal on the both the edges of the clock.

Each lane interconnect provides up to 2.5 Gbps with effective data rate of 10 Gbps.

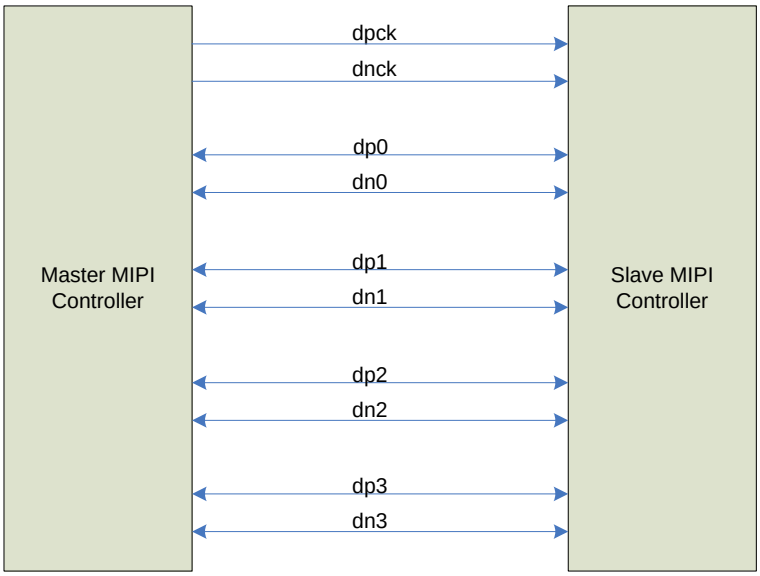

Figure 3: MIPI Link Diagram for DPHY

3.4 D-PHY Lane Architecture

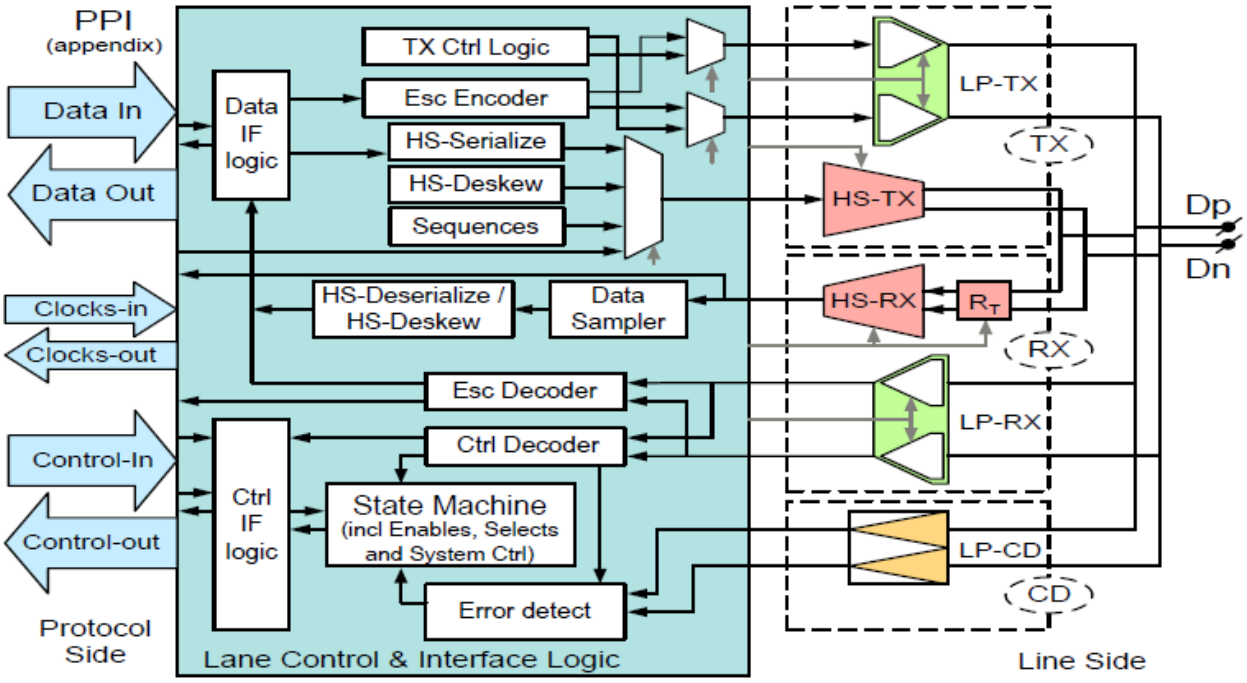

Figure 4: DPHY Lane Architecture

Each Data Lane and Clock Lane Module has a control and interface logic unit and a transceiver portion to handle Differential High-Speed DDR functions, single-ended Low-Power functions operating on each of the interconnect wires individually. The I/O functions are controlled by a Lane Control and Interface Logic block.

High-Speed signals have a low voltage swing of 250 mV, while Low-Power signals have a large swing of 1.2V. High-Speed functions are used for High-Speed Data traffic. The Low-Power functions are mainly used for control and can have data transfer support.

High Speed data width is 8bit at the PPI side, which is serialized and transmitted one bit at a time on each edge of clock lane.

Control and Interface Logic, sends and detects start of packet signaling and end of packet signaling on the data lanes. It has a serializer and de-serializer unit to dialog with the PPI / PHY adapter unit. Also it has clock divider unit to source and receive data during parallel data transfers from and to the PPI.

DPHY provides the de-skew circuits which re-aligns clock lane in exact quadrature relationship with the data lane to match the skew that can occur on the board or packaging.

Note: The Arasan ComPHY combines many modules described in figure 2 and 4. The details are proprietary and is not shown in the data sheet.

3.5 ComPHY Connectivity Details

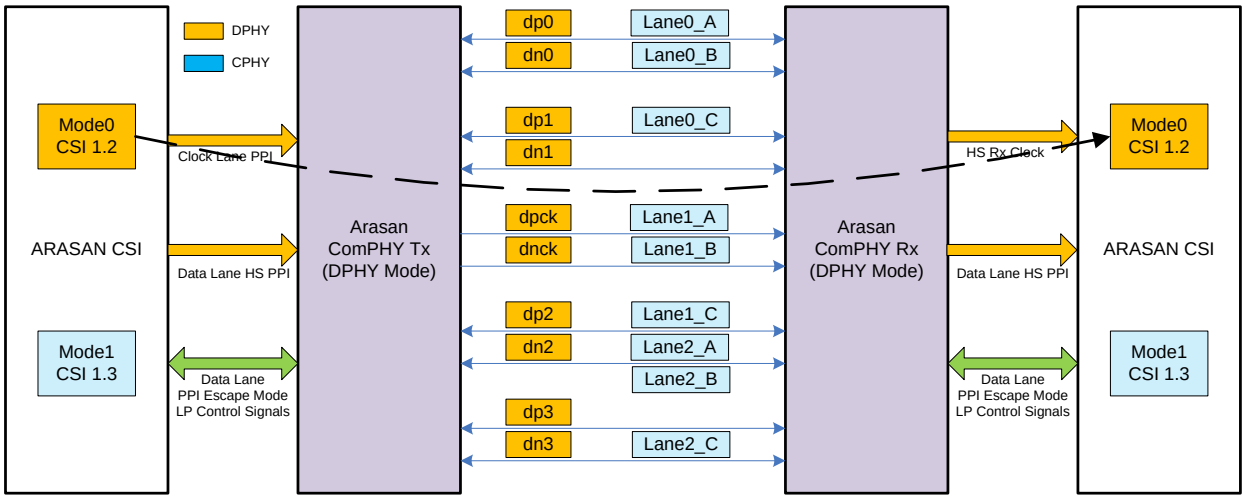

Figure 5:D-PHY Mode

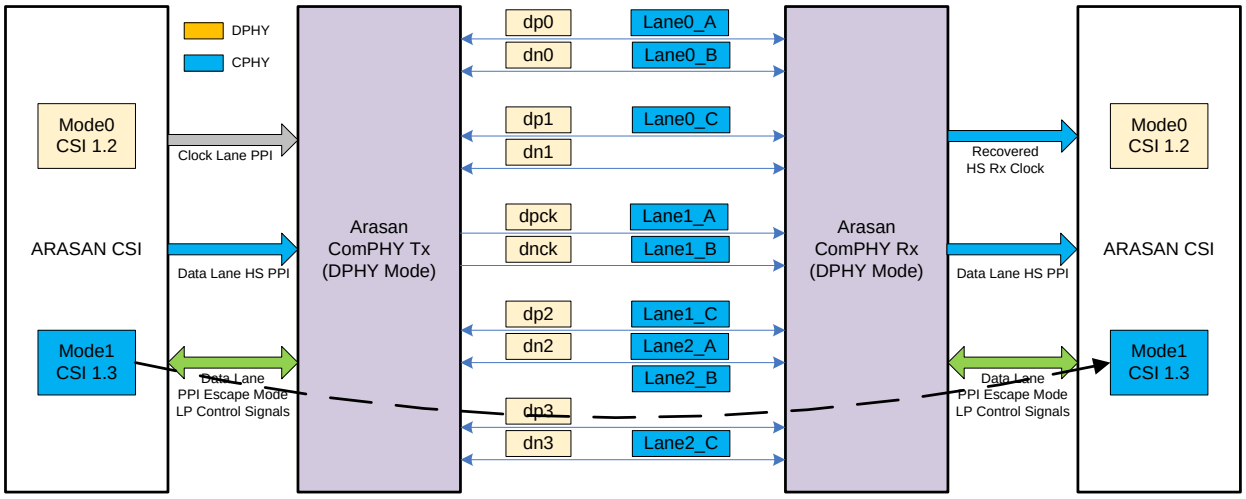

Figure 6: C-PHY Mode

4 Arasan's ComPHY Pad Table

Table 1: Function Description of ComPHY Analog Pads

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dpck / lane1_A	Bidirectional	Positive polarity of low voltage differential clock signal for transmitter and receiver	Wire A in the 3 wire lane of 1st lane
2	dnck / lane1_B	Bidirectional	Negative polarity of low voltage differential clock signal for transmitter and receiver	Wire B in the 3 wire lane of 1st lane
3	dp2 / lane1_C	Bidirectional	Positive polarity of low voltage differential data signal for lane2	Wire C in the 3 wire lane of 1st lane
4	dn2 / lane2_A	Bidirectional	Negative polarity of low voltage differential data signal for lane2	Wire A in the 3 wire lane of 2nd lane
5	dp3 / lane2_B	Bidirectional	Positive polarity of low voltage differential data signal for lane3	Wire B in the 3 wire lane of 2nd lane
6	dn3 / lane2_C	Bidirectional	Negative polarity of low voltage differential data signal for lane3	Wire C in the 3 wire lane of 2nd lane
7	dp0 / lane0_A	Bidirectional	Positive polarity of low voltage differential data signal for lane0	Wire A in the 3 wire lane of 1st lane
8	dn0 / lane0_B	Bidirectional	Negative polarity of low voltage differential data signal for lane0	Wire B in the 3 wire lane of 1st lane
9	dp1 / lane0_C	Bidirectional	Positive polarity of low voltage differential data signal for lane1	Wire C in the 3 wire lane of 1st lane
10	dn1	Bidirectional	Negative polarity of low voltage differential data signal for lane1	

Table 2: Power Pads

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	VDD_clk	Power	Power pad for the clock lane	Power pad for the data lane0
2	VSS_clk	Power	Ground pad for the clock lane	Ground pad for the data lane0
3	VDD_d0d1	Power	Power pad for Data lane 0 and Data lane 1	Power pad for the data lane1
4	VSS_d0d1	Power	Ground pad for Data lane 0 and Data lane 1	Ground pad for the data lane1
5	VDD_d2d3	Power	Power pad for Data lane 2 and Data lane 3	Power pad for the data lane2
6	VSS_d2d3	Power	Ground pad for Data lane 2 and Data lane 3	Ground pad for the data lane2
7	VDDD	Power	Power pad for the DFE	Power pad for the DFE
8	VSSD	Power	Ground pad for the DFE	Ground pad for the DFE

Table 3: Analog Functioning Trimming Inputs

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	trim_0[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
2	trim_1[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
3	trim_2[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY
4	trim_3[31:0]	Input	Trim bits for DPHY	Trim bits for CPHY

Table 4: Clock and Reset Inputs

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	TxClkEsc	Input	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. This is also the input reference clock for the PLL
2	enable	Input	Active Low system reset to the module	Active Low system reset to the module
3	dln_bd_ForceRxmode	Input	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.	Force Lane Module Into Receive mode / Wait for Stop state. This signal forces the state machine into RX mode.

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
4	dln_ForceTxStopmode[3:0]	Input	Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines	Only the first three bits are used for the CPHY. Force Lane Module Into Transmit mode / Generate Stop state. This signal forces STOP signal on the transmit lines

Table 5: Clock lane High Speed PPI interface Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	cln_TxRequestHS	Input	High-Speed Transmit Request and Data Valid for clock lane. For clock Lanes, this active high signal causes the lane module to begin transmitting a high-speed clock	-
2	cln_RxActiveHS	Output	Receiver Clock Active. This asynchronous, active high signal indicates that a clock Lane is receiving a DDR clock signal	-
3	TxByteClkHS / TxWordClkHS	Output	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one transmitter's byte clock signal. The frequency of byte clock is exactly 1/8 the High-Speed bit rate This is the txbyteclkhs to which all PPI interface is synchronous for transmitter.	High-Speed Transmit Word Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. The same clock is shared by all lane modules. The frequency of TxWordClkHS is exactly 1/7 the high-speed symbol rate.
4	RxByteClkHS / RxWordClkHS	Output	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The rxbyteclkhs is generated by dividing the received High-Speed DDR clock This is the byte clock to which all PPI interface is synchronous for receiver	High-Speed Receive Word Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock.

Table 6: Clock, Special Controls and Test Mode Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	cln_TxUlpsExit	Input	Transmit ULP Exit Sequence for clock lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when tx_ulpsactivenot_clk_n becomes de-asserted. txulpsexit_clk is synchronous to txclkesc. This signal is ignored when the Lane is not in the ULP State	-
2	cln_TxUlpsClk	Input	To force the clock lane to transmit ULPS sequences in the clock line	-
3	cln_RxUlpsClkNot	Output	Receive Ultra Low-Power mode on Clock Lane. This active low signal is asserted to indicate that the Clock Lane module has entered the Ultra Low-Power mode. The Lane module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect	-
4	cln_tx_UlpsActive Not	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-
5	cln_rx_UlpsActiveN ot	Output	ULP State (not) Active for clock lane. This active low signal i s asserted to indicate that the Lane is in ULP state.	-

Table 7: Clock Lane PPI Control Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	cln_Rxstopstate	Output	Lane is in Stop state for clock lane. This active high signal indicates that the lane module is currently in Stop state. This is valid for both receivers and transmitters. Note that this signal is asynchronous to any clock in the PPI interface	-

Table 8: Data lane High Speed PPI Interface Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_TxDataHS[47:0]	Input	High-Speed Transmit Data for data lane. high-speed data to be transmitted. Data is captured on rising edges of transmitted byte clock. First 32 bits are only used for DPHY	High-Speed Transmit Data for data lane. high-speed data to be transmitted. Data is captured on rising edges of TxWordClkHS.
2	dln_TxRequestHS [3:0]	Input	High-Speed Transmit Request and Data Valid for data lane. A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on txdatahs_0 to be transmitted. The lane module accepts the data when both dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low	Only first three bits are used for the CPHY High-Speed Transmit Request and Data Valid for data lane . A low-to-high transition on dln_TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on dln_TxRequestHS causes the lane module to initiate an End-of- Transmission sequence. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on dln_TxDataHS to be transmitted. The lane module accepts the data when both dln_TxRequestHS and dln_TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol always provides valid transmit data when txdatahs_0 is active. Once asserted, dln_TxDataHS remains high until the data has been accepted, as indicated by dln_TxReadyHS. dln_TxRequestHS is only asserted while dln_TxRequestEsc is low
3	dln_TxReadyHS [3:0]	OUTPUT	High-Speed Transmit Ready for data lane. This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of transmitted byte clock	High-Speed Transmit Ready for data lane. First three bits only used for CPHY This active high signal indicates that dln_TxDataHS is accepted by the lane module to be serially transmitted. dln_TxReadyHS is valid on rising edges of TxWordClkHS
4	dln_TxSendSyncHS[2:0]	Input	-	High Speed Command to

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
				Transmit Sync Word. This command signal has the same timing as TxDataHS[15:0] on the PPI, but when TxSendSyncHS is active on a given TxWordClkHS cycle then TxDataHS[15:0] is ignored for any Word Clock cycle where TxSendSyncHS is active.
5	dln_RxDataHS[47:0]	OUTPUT	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of receiver byte clock Only first 31 bits are used for DPHY	High-Speed Receive Data for data lane. The signal connected to dln_RxDataHS was received first. Data is transferred on rising edges of RxWordClkHS
6	dln_RxValidHS[3:0]	OUTPUT	High-Speed Receive Data Valid for data lane	High-Speed Receive Data Valid for data lane. Only first three bits are used for CPHY
7	dln_RxInvalidCodeHS[2:0]	Output	-	High-Speed Invalid Code Word Detection. A high-speed status signal that indicates the present word on RxDataHS[15:0] was produced by a group of seven symbols that were not a valid code word.
7	dln_RxActiveHS[3:0]	OUTPUT	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect.	High-Speed Reception Active for data lane. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the lane interconnect. Only first three bits are used for CPHY
8	dln_RxSyncHS[3:0]	OUTPUT	Receiver Synchronization Observed for data lane. This active high signal indicates that the Lane module has seen an appropriate synchronization event. In a typical high-speed transmission, dln_RxSyncHS is high for one cycle of received byte clock at the beginning of a high-speed transmission when dln_RxActiveHS is first	Receiver Synchronization Observed for data lane . This active high signal indicates that the lane module has detected the 7-symbol sync word in the received data. In a typical high-speed transmission, dln_RxSyncHS is high for one cycle of RxWordClkHS at the beginning of a high-speed transmission when dln_RxActiveHS is first

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			asserted, and again for one cycle of received byte clock at the end of a high-speed trans-mission, just before dln_RxValidHS returns low.	asserted, and also prior to redundant packet headers that may appear in the data burst. First three bits are used for CPHY

Table 9: Data lane High Speed PPI Interface Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_TxRequestEsc [3:0]	Input	Escape mode Transmit Request for data lane. dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low.	Escape mode Transmit Request for data lane . dln_TxRequestEsc is only asserted by the protocol while dln_TxRequestHS is low. Only first three bits are used for the CPHY.
2	dln_TxUlpsExit[3:0]	Input	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes de-asserted. dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.	Transmit ULP Exit Sequence for data lane. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark- 1 when ulpsactivenot_0_n becomes de-asserted. dln_TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State. Only first three bits are used for CPHY.
3	dln_TxUlpsEsc[3:0]	Input	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains	Escape mode Transmit Ultra Low Power for data lane. This active high signal is asserted with dln_TxRequestEsc to cause the lane module to enter the ultra low power mode. The lane module remains

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted.	in this mode until dln_TxRequestEsc is de-asserted. dln_bd_TxLpdtEsc and all bits of dln_bd_TxTriggerEsc are low when dln_TxUlpsEsc is asserted. Only first three bits are used for CPHY
4	dln_bd_TxLpdtEsc	Input	This signal is used to request a low power data transmission entry in the forward direction.	This signal is used to request a low power data transmission entry in the forward direction.
5	dln_bd_TxTriggerEsc[3:0]	Input	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction	A 4 bit signal that triggers a trigger sequence in the ESC mode in the forward direction
6	dln_bd_TxDataEsc [7:0]	Input	In data mode, the 8-bit data to be transmitted in the forward direction.	In data mode, the 8-bit data to be transmitted in the forward direction.
7	dln_bd_TxValidEsc	Input	A valid signal which qualifies for the data lines.	A valid signal which qualifies for the data lines.
8	dln_bd_TurnDisable	Input	To avoid the turn around request during the lock up situation	To avoid the turn around request during the lock up situation
9	dln_bd_Direction	Output	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)	To indicate the direction of the data lane. This signal is used to indicate the current direction of the lane interconnect. When direction_0 =0, the lane is in transmit mode (0=Output). When direction_0 =1, the lane is in receive mode (1=Input)
10	dln_bd_TurnRequest	Input	This signal is used to request a Turn around operation for a bi-directional lane	This signal is used to request a Turn around operation for a bi-directional lane
11	dln_rx_RxClkEsc [3:0]	Output	Escape mode Receive Clock for data lane 0. This signal is used to	Escape mode Receive Clock for data lane 0. This signal is used to

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic	transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic. Only first three bits are valid for CPHY

Table 10: Data lane Escape Mode PPI Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_rx_RxUlpsEsc[3:0]	Output	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect	Escape Ultra Low Power (Receive) mode for data lane. This active high signal is asserted to indicate that the lane module has entered the ultra low power mode. The lane module remains in this mode with dln_rx_RxUlpsEsc asserted until a Stop state is detected on the lane interconnect. Only first three bits are used for the CPHY.
2	dln_rx_UlpsActive Not[3:0]	Output	ULPS signal received on the receiver in the bi-directional lane	ULPS signal received on the receiver in the bi-directional lane. Only first three bits are used for the CPHY.
3	dln_bd_TxReadyEsc	Output	Ready signal for the transmit data lines in reverse direction	Ready signal for the transmit data lines in reverse direction
4	dln_rx_RxDataEsc [7:0]	Output	The low power mode data in the Escape mode.	The low power mode data in the Escape mode.
5	dln_rx_RxValidEsc	Output	The ESC mode valid data	The ESC mode valid data
6	dln_rx_RxTrigger Esc[3:0]	Output	The Trigger mode receiver signal	The Trigger mode receiver signal
7	dln_rx_RxLpdtEsc	Output	The low power data transfer for the first lane	The low power data transfer for the first lane
8	dln_rx_ErrEsc	Output	Error on the Escape sequence during receiver	Error on the Escape sequence during receiver
9	dln_rx_ErrSyncEsc	Output	Error in sync esc in the receiver mode	Error in sync esc in the receiver mode

Table 11: Data lane Escape Mode PPI Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_RxStopState [3:0]	Output	Lane is in Stop state for data lane. This active high signal	Only the first three bits are used for CPHY. Indicates Lane is in Stop

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.	state for data lane. This active high signal indicates that the lane module is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface.
2	dln_tx_UlpsActive Not[3:0]	Output	ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.	Only the first three bits are used for CPHY. Indicates ULP State (not) Active for data lane . This active low signal is asserted to indicate that the Lane is in ULP state.
3	dln_ErrorSotHS[3:0]	Output	Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of receiver's byte clock. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.	Only the first three bits are used for CPHY. Indicates Start-of-Transmission (SoT) Error for data lane . If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RxWordClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
4	dln_ErrorSotSync HS[3:0]	Output	Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of receiver's byte clock.	Only the first three bits are used for CPHY. Indicates Start-of-Transmission Synchronization Error for data lane 0. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one RxWordClkHS
5	TxSkewCalHS	Input	Initiate the periodic de-skew burst at the transmitter.	-

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			A low-to-high transition on TxSkewCalHS causes the PHY to initiate a de-skew calibration. A high-to-low transition on TxSkewCalHS causes the PHY to stop de-skew pattern transmission and initiate an end-of-transmission sequence.	
6	RxSkewCalHS	Output	High-Speed Receive Skew Calibration, which indicates the successful de-skew operation to the upper layer.	-
7	dln_ErrContention LP0	Output	Indicates LP0 contention on lane0.	Indicates LP0 contention on lane0.
8	dln_ErrContention LP1	Output	Indicates LP1 contention on lane1.	Indicates LP1 contention on lane1.
9	dln_rx_ErrControl [3:0]	Output	Indicates Error control assertion in corresponding lane	Only the first three bits are used for CPHY. Indicates Error control assertion in corresponding lane

Table 12: ALP supporting Signals for CPHY

	Pins (DPHY/CPHY)	Direction	Description(CPHY)
1	dln_TxSendALPHS[5:0]	INPUT	High-Speed Command to Transmit ALP Code. The protocol adapter attached to the C-PHY may need to transmit ALP Codes. This command signal has the same timing as High-Speed Transmit Data on the PPI, but when a TxSendALPHS signal is active on a given TxWordClkHS cycle then the corresponding 16 bits of High-Speed Transmit Data is ignored and the C-PHY transmits an ALP Code in place of the corresponding High-Speed Data Word for any Word Clock cycle where a TxSendALPHS signal is active. The following Transmit ALP Command signals are defined based on the width of the transmit data path: • 16-bit width – TxSendALPHS[0] • 32-bit width – TxSendALPHS[1:0] The following Transmit ALP Command signals cause an ALP Code to be transmitted as follows:

	Pins (DPHY/CPHY)	Direction	Description(CPHY)
			• TxSendALPHS[0] – transmit an ALP Code in place of the C-PHY mapped version of TxDataHS[15:0] • TxSendALPHS[1] – transmit an ALP Code in place of the C-PHY mapped version of TxDataHS[31:16]
2	dln_TxALPCodeHS0[11:0]	INPUT	High-Speed Transmit ALP Code. When TxSendALPHS[0] is asserted then TxALPCodeHS0[3:0] selects which ALP Code is transmitted. Similarly, When TxSendALPHS[1] is asserted then TxALPCodeHS1[3:0] selects which ALP Code is transmitted. The mapping of the 4-bit TxALPCodeHS0[3:0] and TxALPCodeHS1[3:0] values to the transmitted ALP Codes is specified in CPHY 1.2 Specification ***Table*** 16.The following Transmit ALP Code signals are defined based on the width of the transmit data path: • 16-bit width – TxALPCodeHS0[3:0] • 32-bit width – TxALPCodeHS0[3:0] and TxALPCodeHS1[3:0]
3	dln_TxALPCodeHS1[11:0]	INPUT	
4	dln_TxALPNibble0[11:0]	INPUT	High-Speed ALP Nibble Data. When TxSendALPHS[0] is asserted and TxALPCodeHS0[3:0] = 0b1010 to select the LPDT Nibble Code then TxALPNibble0[3:0] specifies the values of the first and last symbols of the LPDT Nibble Code. Similarly, when TxSendALPHS[1] is asserted and TxALPCodeHS1[3:0] = 0b1010 to select the LPDT Nibble Code then TxALPNibble1[3:0] specifies the values of the first and last symbols of the LPDT Nibble Code. The mapping of the 4-bit Nibble Code to the S1 and S0 symbols is specified in CPHY 1.2 Specification ***Table 16*** and ***Section 6.4.5.4***. The following ALP Nibble Code signals are defined based on the width of the transmit data path: • 16-bit width – TxALPNibble0[3:0] • 32-bit width – TxALPNibble0[3:0] and TxALPNibble1[3:0]
5	dln_TxALPNibble1[11:0]	INPUT	
6	dln_RxALPValidHS[5:0]	OUTPUT	Receiver ALP Code Observed. These active high signals indicate that the Lane Module has detected the 7-symbol ALP Code in the received data. In a typical High-Speed transmission, RxALPValidHS[0] is high for one cycle of RxWordClkHS whenever a valid ALP Code is received in a High-Speed burst following the normal preamble or following the calibration preamble. The following Receiver ALP Code Observed signals are defined based on the width of the receive data path: • 16-bit width – RxALPValidHS[0] • 32-bit width – RxALPValidHS[1:0] The following Receiver ALP Code Observed signals indicate where an ALP Code was received as follows: • RxALPValidHS[0] – an ALP Code was received and RxDataHS[15:0] does not contain valid received data

	Pins (DPHY/CPHY)	Direction	Description(CPHY)
			• RxALPValidHS[1] – an ALP Code was received and RxDataHS[31:16] does not contain valid received data
7	dln_RxALPCode0[3:0]	OUTPUT	Receiver ALP Code Value. When RxALPValidHS[0] is asserted then RxALPCode0[3:0] indicates which ALP Code was received. Similarly, When RxALPValidHS[1] is asserted then RxALPCode1[3:0] indicates which ALP Code was received. The mapping of the 4-bit ALP Code value to the actual ALP Code is defined in CPHY 1.2 Specification ***Table 16*** with additional descriptions in ***Section 6.4.5***. The following Receiver ALP Code Value signals are defined based on the width of the receive data path: • 16-bit width – RxALPCode0[3:0] • 32-bit width – RxALPCode0[3:0] and RxALPCode1[3:0]
8	dln_RxALPCode1[3:0]	OUTPUT	
9	dln_RxALPNibble0[3:0]	OUTPUT	Receiver ALP LPDT Nibble Data. When RxALPValidHS[0] is asserted and RxALPCode0[3:0] is equal to 0b1010 (which corresponds to the LPDT Nibble Code) then RxALPNibble0[3:0] contains four bits of valid LPDT data. Similarly, When RxALPValidHS[1] is asserted and RxALPCode1[3:0] is equal to 0b1010 (which corresponds to the LPDT Nibble Code) then RxALPNibble1[3:0] contains four bits of valid LPDT data. The definition of the format of the LPDT nibble data within the ALP code is defined in CPHY 1.2 Specification ***Table 16*** and ***Section 6.4.5.4***. The following Receiver ALP LPDT Nibble Data signals are defined based on the width of the receive data path: • 16-bit width – RxALPNibble0[3:0] • 32-bit width – RxALPNibble0[3:0] and RxALPNibble1[3:0]
10	dln_RxALPNibble1[3:0]	OUTPUT	
11	dln_ALPWakeState[8:0]	INPUT	ALP-Pause Wake Wire State A group of control signals that select the wire state to be driven on the Lane during the ALP-Pause Wake state. The default is to drive the “+x” state but it may be necessary to drive one of the other five possible states to resolve wire permutations in the Lane Interconnect, in case A, B and C at the Master are not connected to A. B and C, respectively, at the Slave. The binary values on ALPWakeState[2:0] choose the wire state driven during ALP-Pause Wake as follows: • 000 – “+x” driven during ALP-Pause Wake (default) • 001 – “-x” driven during ALP-Pause Wake • 010 – “+y” driven during ALP-Pause Wake • 011 – “-y” driven during ALP-Pause Wake • 100 – “+z” driven during ALP-Pause Wake • 101 – “-z” driven during ALP-Pause Wake

Table 13: Side Band Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_def_dir	Input	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.	Provides the default direction of the bi-directional lane, 1'b1-receive, 1'b0-transmit.
2	cln_pll_locked	Output	Pll locked signal from the Dphy	Pll locked signal from the Dphy

Table 14: Clock lane PPI Control Signals

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
1	dln_cnt_hs_prep[7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
2	dln_cnt_hs_zero[7:0]	Input	The period for which HS prepare time should be accommodated for data lane in Byte clock period	The period for which HS prepare time should be accommodated for data lane in Word clock period
3	dln_cnt_hs_trail[7:0]	Input	The period for which HS Trail time should be accommodated for data lane in Byte clock period	The period for which HS trail time should be accommodated for data lane in Word clock period
4	dln_cnt_hs_exit[7:0]	Input	The period for which HS Exit time should be accommodated for data lane in Byte clock period	The period for which HS exit time should be accommodated for data lane in Word clock period
5	dln_rx_cnt[7:0]	Input	Counter that controls the assertion of enable on the DPHY for data lane in Byte clock period	Counter that controls the assertion of enable on the DPHY for data lane in Word clock period
6	dln_sync_cnt[7:0]	Input	A timeout value used for sync error detector logic for data lane in Byte clock period	A timeout value used for sync error detector logic for data lane in Word clock period
7	dln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period	The time period in which LP states are driven in Byte clock period
8	cln_cnt_hs_trail[7:0]	Input	The period for which HS trail	-

No.	Pins (DPHY/CPHY)	Direction	Description (DPHY)	Description (CPHY)
			time should be accommodated for clock lane in Byte clock period	
9	cln_cnt_hs_exit[7:0]	Input	The period for which HS exit time should be accommodated for clock lane in Byte clock period	-
10	cln_cnt_lpx[7:0]	Input	The time period in which LP states are driven in Byte clock period for clock lane	-
11	cln_cnt_prep[7:0]	Input	The period for which HS prepare time should be accommodated for clock lane in Byte clock period	-
12	cln_cnt_zero[7:0]	Input	The period for which HS zero time should be accommodated for clock lane in Byte clock period	-
13	cln_cnt_pll[15:0]	Input	The count value which is used for the PLL lock time	The count value which is used for the PLL lock time

Note: This is hard IP – Pinout is subject to change depending on process node, features and so on.

5 Hard Macro Deliverables

- GDS-II
- CDL netlist for LVS
- LVS reports
- DRC and Antenna reports
- LIB files
- User guide and Integration Guides
- LEF
- Scan-inserted netlist for DFT
- Verification Environment with behavioral models
- IBIS Models