Comprehensive Portfolio for TSMC 22nm

MIPI C-PHY℠, MIPI D-PHY℠ 1.1, MIPI D-PHY℠ 1.2 and eMMC™

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All about TSMC 22nm

In accordance with Moore's law, over the time transistors are becoming smaller and smaller thereby making the computing and communication devices smarter and highly efficient. Keeping up with the ever-shrinking size of the transistors has not been easy and thus came the need of transitioning from planar bulk CMOS (28nm) to 3D FinFET (16nm/14nm and beyond) technology. However, the strong desire to migrate from 28nm to 16nm/14nm FinFET which is ideal for high performance applications, comes with high costs of IC architecture that is not acceptable by all businesses and has limitations for applications in the field of IoT and mixed signals. Hence comes the persuasive TSMC 22nm technique, a node which provides a balance between the performance and cost. The TSMC 22nm technology is ideal for businesses/applications requiring better performance than 28nm but also not wanting to pay the higher costs for 16nm/12nm and beyond on FINFET.

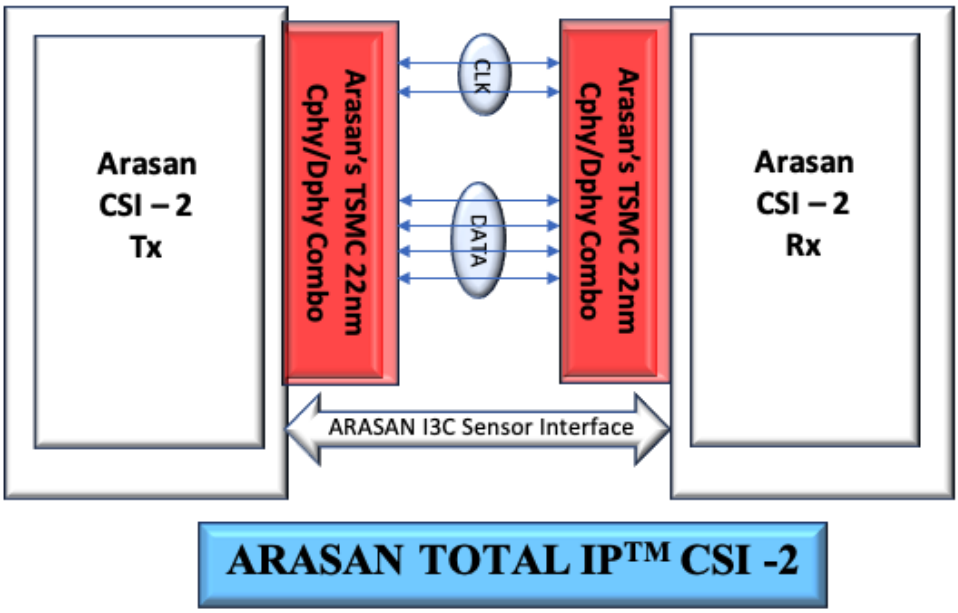
The TSMC's Ultra low power 22nm technology (22ULP) was developed with TSMC's industry-leading 28nm technology and in the fourth quarter of 2018 achieved all process qualifications. Compared to 28 nm (28 HPC) of lightweight high quality, 22 ULS offers 10% reduced area for applications such as image processing, digital TV, Set-top boxes, smartphones and consumer goods with a speed increase of over 30 percent, or a power reduction of over 30 percent.

Creation of technologies with 22nm ultrasound low leakage (22ULL) has completed and started development of IoT and wearable appliances in the fourth quarter of 2018. The latest ULL and ULL SRAM systems will deliver less power compared to 40ULP and 55ULP (static, Random Access Memory).

At Arasan Chip Systems, Total IP™ all the leading IP's are now available for TSMC's 22nm such as high-speed interfaces like MIPI C-PHY℠, MIPI D-PHY℠ 1.1 and MIPI D-PHY℠ 2.1 and also EMMC™ SD/IO.

MIPI C-PHY^{SM}

The MIPI C-PHY^{SM} interface is a modern synchronous digital networking bus for applications such as smartphones, augmented reality headsets and the Internet of Things platforms, which is usable in high-speed, low-speed applications. The MIPI C-PHY^{SM} norm creates a generic solution for transferring data with high throughput per physical conductor, which makes the device very special in contrast with conventional wireless buses. In addition to circuit-level strategies and concerns for applying this revolutionary scheme, the principle of three-phased encoding has been implemented, along with higher mapping criteria and some ramifications for protocol levels, including fast clock recovery and effective sideband signaling for unmapped terms. With this realization, MIPI C-PHY^{SM} is the embodiment of an evolving digital bus class conventional signal, that incorporates the advantage of single-ended and differential signals in order to retain a low pin count without losing electromagnetic noise immunity.



Arasan's MIPI C-PHY^{SM} IP Core is fully compliant to the MIPI C-PHY^{SM} specification Version 1.2 while also being compliant to the D-PHY^{SM} 1.2 Specification. It supports the MIPI® Camera Serial Interface (CSI-2) and Display Serial Interface (DSI-2) protocols. It is a universal PHY that can be configured as a

transmitter, receiver or both. This IP core is specially optimized for area and power. The MIPI C-PHY℠ is targeted toward high resolution displays to more efficiently transfer data with lower power consumption and die size compared to the D-PHY℠. It utilizes a lower signal rate than the MIPI D-PHY℠ but provides support for low-cost, low-resolution image sensors, sensors offering up to 60 megapixels; and 4K video display panels.

Arasan's MIPI C-PHY℠ v1.2 achieves a peak bandwidth of 3.5 Gb/s at 2.28 bits/symbol, or 17.1 Gbps over a 9-wire interface, compared to the MIPI D-PHY℠ v1.2 peak transmission rate of 2.5 Gbps/lane or 6 Gbps over a 10 wire - 4 lane interface.

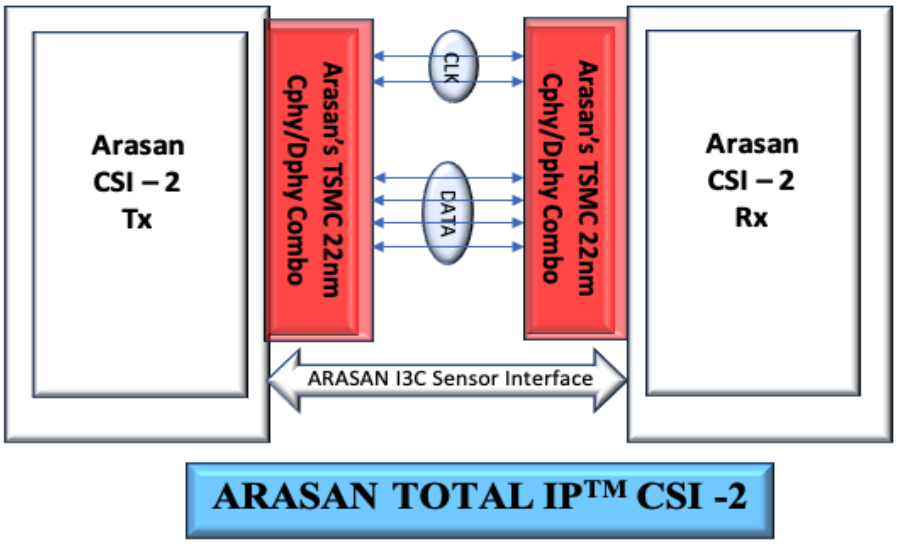
Arasan's MIPI C-PHY℠ is immediately available for the TSMC 22nm which is verified, and silicon proven for Arasan Total IP™ for MIPI camera interface CSI-2® and MIPI display interface DSI® and DSI-2®. Arasan's MIPI C-PHY℠ is also available in 28nm and 16nm processes.

MIPI D-PHY℠ 1.1 and 1.2

MIPI D-PHY℠ binds high-resolution cameras and screens to a processor. It's a synchronous clock-forwarded connection with high immunity to noise and a high resistance. MIPI D-PHY℠ makes low latency switches between low and high-speed modes.

Since it offers a flexible, high-speed, low-power and low-cost solution, it is an in demand PHY for cameras and displays on smartphones. It is also used in many other uses, including helicopters, large smartphones, surveillance cameras and industrial robotics. MIPI D-PHY℠ is still used extensively in vehicle applications with the help of patented bridging solutions, including camera sensing devices, radar collision prevention, in-car infotainment and dashboards.

Due to the master-slave relationship of the connection transceivers, service and data rates required for a link are asymmetrical. For the monitor and camera use cases with one main data transmitting path, the asymmetric architecture greatly reduces the difficulty of the connection. The operation is optional, bi-directional and half-duplex.



ARASAN TOTAL IP™ CSI -2

At Arasan Chip Systems, MIPI D-PHY℠ v1.1 IP with supporting speed of up to 1.5 Gbps and MIPI D-PHY℠ v1.2 IP with supporting speed of up to 2.5 Gbps, is available immediately for the TSMC 22nm process technology. The MIPI D-PHY℠ IP is further optimized for lower power targeting wearables and IoT Display applications which require low throughput for their small lower resolution screens, but where power is of paramount importance.

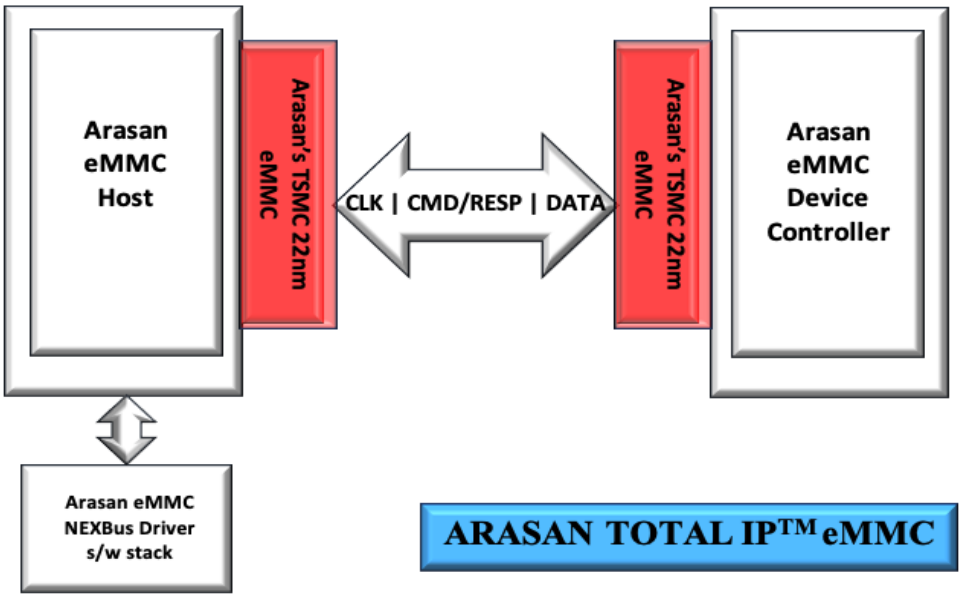
The MIPI D-PHY℠ IP is also available as a Tx only IP for companies looking to save silicon area and further improve power consumption. The MIPI D-PHY℠ IP on TSMC 22nm is seamlessly integrated and verified with Arasan's own MIPI DSI℠ Tx and MIPI DSI℠ Rx IP cores as part of its Total IP™ MIPI Display interface for wearables and IoT.

eMMC™

If something has been revealed to us about technological development in the last two decades, there is still desire for more. In order to satisfy these criteria, better goods are required. Some days, without keypads or with a multimedia library covering hundreds of gigabytes you might not even picture a smartphone.

Faster connections also improved media use with high definition and specialized telephone cameras to produce them. You can now shoot 4K images and save massive files in minutes on smartphones. In smartphones around the

world, eMMC is the most used storage option. In terms of performance, the read speed of 140MB/s in eMMC 4.5 to 250MB/s in eMMC 5.1 is improved.



Arasan's 22nm eMMC™ Total IP™ has general purpose I/O PADs that are multipurpose PADs which can be programmed to operate in different modes: 1) Output with predetermined source/sink impedance, 2) Open drain, 3) Input, 4) Tristate and 5) Weak pull up or pull down. The I/O PADs are specially designed to seamlessly integrate with Arasan's eMMC™ 5.1 IP.

Arasan introduced the industry's first eMMC™ in 2013 on TSMC 28nm node and later on 16nm node which can be made available immediately. Arasan will deliver eMMC PHY on TSMC 5nm and will be made available as part of its Total IP™ eMMC 5.1 Solution.