Enabling Technology Adoption through Total IP Solutions

By
Somnath Viswanath – Product Marketing Manager

January, 2010

Arasan
The Bus Stops Here

Introduction

The increasing complexity and time to market pressures faced by SoC/System design teams necessitates them to look at things from a system perspective. Current SoC architectures resemble entire systems of prior generations, integrating multiple compute engines, hardware logic, memory interfaces and a myriad of bus interfaces. This increase in SoC complexity has resulted in verification becoming the bottleneck in the pre-silicon phase, while software drivers and system validation become the gating items in the post silicon phase.

As a result of these competitive pressures semiconductor companies are increasingly leveraging the Intellectual Property ecosystem to source standard Bus IP cores and other IP, while focusing in-house resources on implementing proprietary features that result in a competitive advantage. Standard bus interfaces between a SoC and peripheral chips are a logical starting point for vendors like Arasan Chip Systems.

While traditionally RTL (hardware) IP providers were focused solely on providing an RTL database for their IP, SoC designers prefer a to source all IP collateral such as EDA scripts, verification IP, software stacks, and validation systems from one vendor. In this paper we discuss the recent trend in SoC design practice to source all IP collateral from the same vendor so as to lower risk and speed up time to market, reducing their overall development time.

SoC Design today

SoC design teams are constantly exploring options to improve productivity while reducing cost. An increasing number of design teams are now relying on design automation tools as well as third-party IP to leverage their internal design effort. This has resulted in a healthy ecosystem for competitive sources of IP. Market pressures have resulted in even large OEMs and Fabless semiconductor companies to pursue a SoC development strategy that relies on external IP providers rather than use internal teams to design standards based IP.

With the increasing use of third-party IP, the overhead of managing, qualifying and successfully integrating these IP's has meant that design teams now spend significant amounts of time dealing with IP related issues. More often than not, the time and effort spent in these activities are not predictable in the project budget and schedule.

In the pre-silicon world, customizing, integrating, debugging and verifying a SoC implementation that includes IP from multiple sources, can lead to schedule overflows while trying to co-ordinate with these multiple vendors and dealing with the verification process and tools. This problem is compounded at the system-level (post silicon world), thus requiring Hardware validation platforms and integration of software drivers (interfacing to the hardware architecture layer) and Stacks (interfacing to the operating system environment).

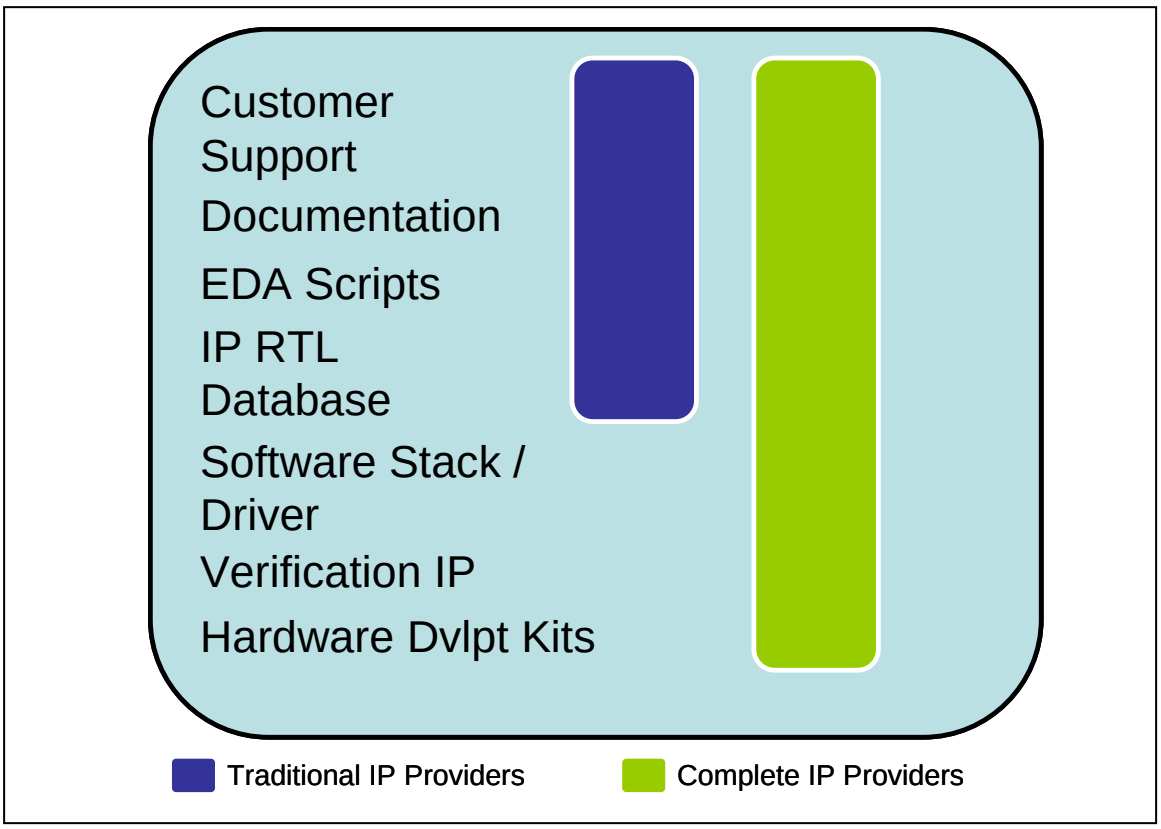

Figure 1. The growing scope of IP collateral necessary for successful IP integration into a SoC.

In response to these trends, enabling technology adoption has become the key focus for semiconductor IP providers. These providers are expanding the components provided with each IP to not only include the RTL IP core database but also verification IP environments and to facilitate post silicon design activity by supplying system-level software development and hardware platforms for SoC integration (see Figure 1). The supporting collateral together with the base IP are necessary to contain the growing complexity of SoC architectures while realizing the benefits of integrating third-party IP.

Sourcing all these components from one vendor alleviates the inter-operability between the components while mitigating system design risks.

Benefits of Providing Complete IP Collateral

While many IP vendors continue to focus on providing synthesizable RTL and associated documentation, SoC teams are demanding an increase in scope of deliverables from their IP suppliers. Progressive IP vendors now provide a comprehensive set of hardware and software IP with associated verification environments for their portfolio of products. Sourcing all components needed to successfully use an IP in a SoC design saves considerable design effort while improving the quality of the final solution.

IP Database

The most important value proposition of the IP ecosystem is in providing a thoroughly validated IP core. Providing a verified, high-quality, synthesizable RTL database is the basic starting point for integrating this functionality into a SoC. Adherence to a rigorous RTL coding style and following DFT guidelines is key to preventing incompatibilities with downstream integration and processing by EDA tools. High quality documentation and integration guides are equally important in overcoming the initial effort of integrating the IP with the rest of the SoC design database. Design teams benefit from not only a reduction in design complexity, but also enjoy the benefit of using pre-verified IP to bring their products to market quickly.

EDA Scripts

IP providers invest considerable resources in learning the nuances of the protocols that they then implement in RTL. This domain expertise can be leveraged in providing carefully tuned EDA scripts that guide the implementation from front-end RTL to physical databases. IP vendors that qualify their IP through common industry design flows provide design teams an additional confidence of not having to deal with incompatibilities with downstream EDA tool or encounter flow related limitations. SoC integrators can use these scripts to save effort by avoid time-consuming iterative creation of timing and other design scripts thereby speeding up their design schedule.

Verification IP

The protocol domain expertise developed by IP design teams can be used to provide a comprehensive, hierarchical test-bench that eases IP integration while boosting confidence in the SoC architecture. Pre-silicon verification can overwhelm the resources of in-house SoC teams and providing this collateral is key to helping these teams to converge on their functional verification faster. Verification IP (ViP) enables the SoC design team to leverage the deep protocol expertise of the IP provider to speed up their functional verification. ViP drastically reduces the verification complexity of the SoC design and is a primary means of gaining confidence in the protocol compliance of the IP.

Hardware Development Platforms

The growing complexity of interface protocols make their verification an extremely complex task. The interface IP acts as a bridge between the external world and the SoC. Thorough verification of this interface IP across all system modes and features is a time consuming and complex tasks. These tests can be done more efficiently using a Hardware Development Kit (HDK). The HDK benefits complex system-level validation and speeds up the convergence of the SoC architecture at the platform level.

Software

While the standardization of interface protocols has eased interoperability between the SoC and other peripheral chips, it has however resulted in the increase in complexity of protocol software stacks. This complexity adds yet another factor to the development schedule and resources for a project. At the system-level, software development has emerged as the main bottleneck standing between validated silicon and the delivery of a complete system solution. By providing proven software stacks that are verified to work with the IP, SoC teams benefit by being able to quickly deliver a system-level solution while reducing complexity of the software development effort.

Customer Support

Building upon the collateral offered by the IP vendor is the requirement to offer high quality customer support especially during the crucial phases of the SoC project's milestone such as integration, pre-silicon validation, physical design and post-silicon bring-up. An IP vendor that provides high quality support to enable the SoC project to be successful versus those that just focusing on the immediate IP deliverables will benefit from strong customer relationships leading to more sustainable business. Quality customer support is crucial to SoC teams faced with the task of integrating complex interface protocols on which they might not have in-house expertise.

Benefit of a Total IP Solution

Sourcing IP from a vendor that provides complete IP collateral which has been verified to work together, vastly improves the quality of the SoC design resulting in the faster convergence of the design database. It also bounds and reduces the number of vendors that the SoC team has to interface with, greatly simplifying SoC program management effort. Even simple inter-operability issues between components sourced from two different vendors have been known to throw an entire project timeline into jeopardy.

SoC teams can better utilize in-house resources to implement features that differentiate their product while leveraging the domain expertise of IP providers. This results in the reduction of verification effort and helps bring new products to market quickly.

By offering all of the components of an IP to form a Total IP Solution as suggested in this paper, IP providers can better support SoC teams in their quest for higher levels of integration despite shortening project schedules and dwindling in-house resource. This frees up SoC design teams to focus their in-house resources on implementing differentiating features while leveraging the highly specialized ecosystem of IP providers. By using pre-verified IP with proven verification IP and software stacks, SoC teams are able to improve design productivity while continuing to bring innovative products to market.

Conclusion

With the increasing levels of integration and tighter execution constraints faced by SoC teams, semiconductor companies are constantly examining their entire design cycle to identify methods to leverage external ecosystem partners. Using third-party IP for standard bus interfaces is now an accepted practice. In order to successfully execute an SoC project requires components beyond the IP itself, in particular SoC teams need verification IP, hardware validation platforms and software stacks.

OEMs and Fabless semiconductor companies are therefore demanding an increase in scope of collateral from their IP vendors. Sourcing all of these components for a particular IP from one vendor not only reduces the purchasing and qualification effort but also greatly improves speed and quality of the SoC design.

As a result, IP providers must provide verified hardware and software collateral for standard bus interfaces IP as a means to enhance their value in response to the evolving SoC business model. Semiconductor IP companies are an established part of the SoC design ecosystem and are critical to the success of the latter. The evolution of IP companies to provide verification and software collateral is the next logical step to increase their value in the SoC design chain.

Arasan Chip Systems Inc.

2010 N. First Street, Suite 510, San Jose, CA 95131

Phone: 408-282-1600
Fax: 408-282-7800
Email: sales@arasan.com

Data Sheets Link:

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