Implementing an SD 3.0 Physical Layer

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Arasan
The Bus Stops Here

Overview

Secure Digital (SD) is a non-volatile memory card format developed for use in portable devices. It is widely used in a wide variety of products including digital cameras, digital camcorders, hand-held computers, notebook computers, PDA, media players, mobile phones, GPS receivers, and video game consoles.

Designers of products containing an SD interface will discover that their applications are implemented fastest, at lowest risk and lowest cost by using Intellectual Property (IP) products. For years engineers have gained huge advantages by focusing on their value-added application and licensing the standards interface controllers. Using IP in designs allows engineers to focus on their value-added application.

Arasan SD IP Products

Arasan offers many versions of the SD digital controller designed to suit nearly all applications. In addition the company offers both a Physical (PHY) layer product as well as a driver firmware. Each piece of the SD solution is guaranteed to work with the others. Collectively the products comprise a seamless and complete solution.

The SDIO PHY Challenge

Perhaps in no other aspect is the difficulty of implementing the specification more than in the physical layer. The SD 3.0 specification calls for a data transfer rate of 800 MBits which is achieved over eight data lines using both clock edges at a frequency of 50 MHz.

Clocking bidirectional data at that frequency entails exact control of the timing relationship between the clock and all the data lines. The clock edges sample the data optimally when the edges correspond with the center of the data cycle.

However the clock edges and data may be skewed by changes in temperature and variations is wafer processing enough so that data is captured intermittently or not at all. Some data lines may work while others are inconsistent resulting in CRC errors. What is needed is a design for the PHY that allows reliable data capture by controlling the clock-to-data timing.

The Arasan SD 3.0 PHY Solutions

The Arasan PHY products complement the entire SD 3.0 portfolio and are silicon-proven, synthesizable digital and analog designs that are implemented using standard cell libraries. The PHY has been implemented in 40 nm and 90 nm technologies.

Several solutions are available for implementing PHY solutions. The DLL PHY design uses a tapped DLL to tackle the skew problem as shown in Figure 1.

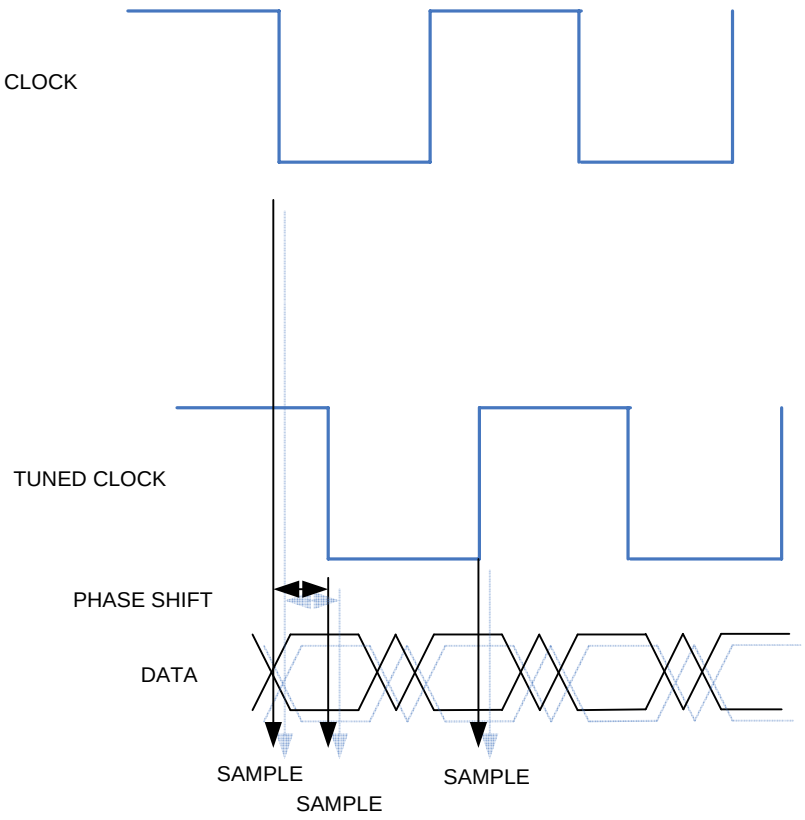

Figure 1: Clock Tuned for Valid Data Sampling

The DLL was designed by Arasan engineers from standard cell library components. The DLL has up to 16 taps each adjusting or tuning the skew of the clock relative to the data up to a maximum of 90 degrees. By experimentation, one can determine which taps to use to shift the phase of the clock so that it reliably captures the data.

The DLL suffers from the requirement to tune the clock on each device manufactured to account for wafer fabrication variations. In addition it may have difficulty accounting for variations in temperature that appear during operation.

Two other methods offer more sophisticated clocking techniques than fixed tuning. The auto tuning method uses a state machine to send and receive a training sequence pattern to continuously monitor the phase relationship between the clock and data. Auto tuning uses feedback from the comparison to adjust the phase relationship to accurately capture data. The method allows for reliable DDR data capture up to 50 MHz and SDR to 100 MHz.

Auto tuning offers the benefit of automatic phase locking at a range of up to 360 degrees, but it suffers from the drawback of wasting power by requiring the state machine to operate continuously.

The PLL method allows the designer to multiply and divide the source clock to any other frequency and then used delay elements to generate eight separate clocks separated by eight equal phases. Any of the phases can be used to synchronize the clock.

The PLL design is a Verilog netlist of components from the standard cell library. The benefit of using the PLL is that it does not run constantly and reduces power consumption. A disadvantage to the method is that the granularity of the lock is only one eighth of an entire clock cycle.

The Host supplies the clock to the Device and so Host-to-Device data transfers do not require being de-skewed. Data coming to the Host, however, can be skewed.

The de-skew process takes place between the Host ad Device when the Host sends a command to the Device to send a known data pattern back to the Host. The 128 byte pattern is stored on both sides and is designed to be susceptible to skew errors. As the Host reads the data it compares it to the known pattern to detect errors. Errors cause the Host to adjust the clock phase by one of the methods described above. The Host will traverse the skew range completely to seek the range over which the data is correct and set the phase in the center of that range.

Summary

Arasan offers several techniques for clock domain synchronization as part of the Total Solution for implementing SD. By licensing the SD 3.0 PHY customers can avail themselves any of these proven solutions.

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