Complete NAND Flash Solution: Logic, PHY and File System Software

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Arasan
The Bus Stops Here

Overview

NAND FLASH memories are non-volatile, inexpensive and of high capacity. These characteristics make these devices ideal for fulfilling the storage requirements in the exploding mobile device market.

Designers using NAND FLASH devices should follow the ONFI standard interface to ensure that their controller design will operate with devices from any vendor. The memories need both digital and analog interfaces between the devices and the system they serve.

When designers add NAND devices to the system design they must consider the least expensive and lowest risk means of implementing the controller.

Trends & Adoption

Device developers need a means of implementing complex controllers for standard interfaces and devices such as NAND memories. In recent years many designers have licensed IP cores for this purpose. The cores are verified to compliance with the standard and are less costly to license than to build. Licensing cores is also the quickest way to add the standard interface to the design.

The Basic Solution

Once the decision is made to license the NAND FLASH controller module the designer should consider IP different vendor's products. The NAND FLASH, for example, requires at lease one digital core for the data transfer control and processor interface and one analog or digital core for the Physical Layer interface (PHY). Software support will also be required in adding NAND Flash to a SoC design. Purchasing the IP cores and the software is probably the most cost effective means of implementation.

When licensing multiple IP products that interact in the system it is wise to consider whether there will be compatibility issues and who will resolve them.

Other drawbacks to licensing IP can include ease of customization to the application, vendor support and testing to ensure compliance.

The PHY portion of the FLASH controller presents its own issues. Unlike many protocols the NAND interface has no framing of data transfers with which to synchronize transfers.

Arasan NAND FLASH Controller Total Solution

Arasan offers a complete solution to the implementation of a NAND FLASH. Developers can license the NAND and PHY controllers together as well as the File system Software for a seamlessly integrated solution. All the products are compliant with latest ONFI Flash Interface specification

The NAND "Total IP Solution" also includes RTL source code, synthesis scripts, test environment and technical documentation.

Among its many features the controller supports error correction and detection schemes and memories up to 128GB with a variety of page sizes. It also supports all mandatory commands and selected optional commands Speeds may range from 40MB/s to 200MB/s to balance performance and power. The controller architecture is shown in Figure 1.

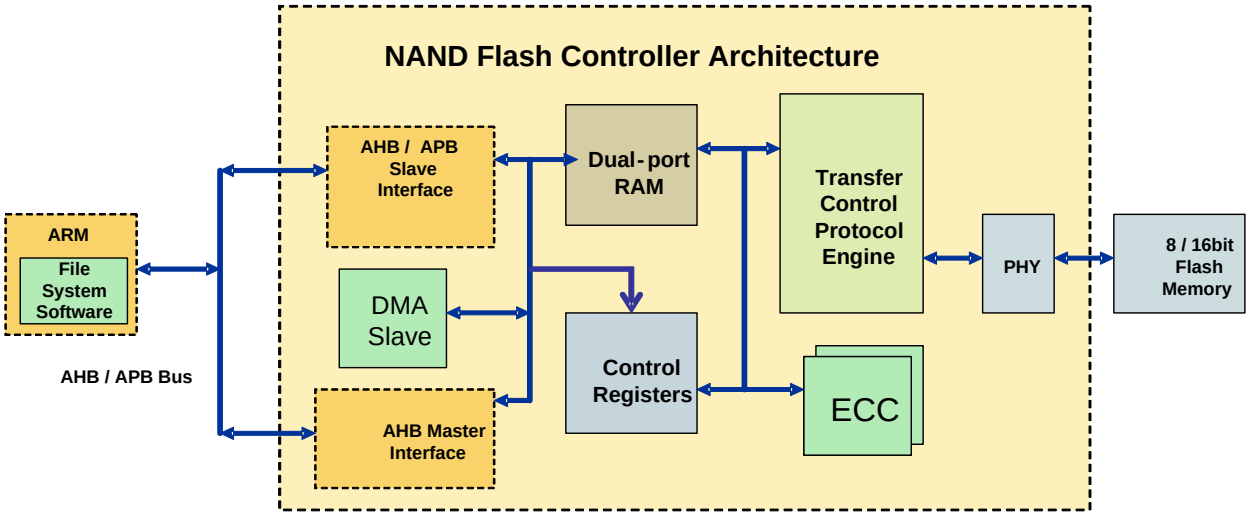

Figure 1: NAND Flash Controller Architecture

The figure shows the controller with an AHB bus interface to the processor. Many other interfaces are also available. The control registers hold configuration information written by the processor. The ECC provides one bit correction and two bit Hamming code error detection and correction for the SLC memory and

The File system Software provides an interface between the OS and Flash controller. The interface guarantees safe data and uncorrupted file system in the event of a power failure.

The File system software also provides garbage collection to reclaim discarded blocks. The software ensures wear leveling so that blocks are evenly utilized which prolongs memory life. The software detects bad memory blocks and maps them out so that the controller does not attempt to use them again. Mapping out reduces error rates.

The PHY layer offers a special challenge to interface designers because of the requirement to sample data synchronized to a clock that is not local. In many communication protocols there is a known series of transitions, usually in the preamble or header that the PHY can synchronize to on incoming packets. NAND FLASH transfers are memory data only and lack a packet structure so there is no sequence to synchronize to.

The synchronization problem is resolved by performing dummy data transfers of patterns of ones and zeros that are not easily locked to and allow the PHY to synchronize to the data stream. The NAND memory cannot be used for this data as there is no way to know what resides there on power initialization.

The solution is for the host to issue a command to the device card to auto tune to the preset pattern contained in a register. The command is issued successively so that the card may

iterate to the optimal solution. During each iteration the card compares the register data with the incoming data. The card shifts the phase by changing the delay line taps to increase or decrease the delay. When the pattern matches the register contents, the delay is tuned.

Different solutions are offered depending on the implementation technology. For an FPGA, Arasan offers a PLL design that samples the incoming data and strobe using different phases of the local clock. The calibration occurs during power-up and ensures valid data as long as power remains.

The benefit of the PLL solution to data synchronization is that it allows use of any clock source which the PLL will be phase aligned to the strobe.

In standard cell technologies two other methods of synchronization are used. One is the DLL method. Here the incoming clock is divided into eight phases. The data and strobe are sampled on the different phases and the phase that offers the most reliable data is used thereafter.

Finally there is the delay line technique in which a delay line is used to delay the strobe signal relative to the clock during read timing. Process variations, however, can cause the delay to be imperfect and so a FIFO is added to the data path to re-synchronize data to the internal clock.

Summary

In offering a “Total IP Solution” Arasan alone provides a complete product whose pieces flawlessly integrate an entire NAND FLASH system. The system includes a PHY, digital controller and software file system.

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