

# Complex Standards Demand New Approaches to IP Quality

## Executive Summary

At Arasan Chip Systems, a world leader in providing standards-based Total IP Solutions for storage and connectivity, the primary benchmark for measurement of quality requires that we answer these questions: Do the IPs work in our customers' SoC? Were they easily integrated into their design? And did they meet the delivery schedule? Our mission is to deliver high quality IP solutions with a commitment towards zero defects through continuous quality improvement.

Gone are the days when the quality of IP was just measured by code and function coverage metrics. Today, the standards take years to finalize and complexity of the IP supporting these standards is equivalent to a complete SoC from just a few years ago with hundreds of thousands of gates, a complex Analog PHY IP operating in the gigahertz range, and software/firmware that is tightly coupled with the Operating System. All have to work together for a smooth operation. Being a standards-based peripheral IP company, Arasan has to ensure that this sub-system interoperates with products that interface to the SoC.

How do we achieve high quality with complex IP spanning digital logic, high-speed mixed signal I/O and software? We achieve this by providing a fully validated total IP solution and working closely with our customers during SoC integration and validation process. This ensures that their ASIC works right first time. We have made and continue to make a significant investment in tools, design and verification methodology and work closely with customers to meet their acceptance criteria. We establish process flows to validate functionality, compliance and mixed-mode operation at a sub-system level. We invest in maintaining deep expertise with the standards committees for MIPI, JEDEC, SD and others. And we work closely with an eco-system of partners like Agilent and Cadence.

In this whitepaper, I will briefly review our methodology using our UFS products as a reference. This is a comprehensive suite that combines the digital UFS host and device controllers, the UniPro<sup>SM</sup> interface technology, the MIPI M-PHY mixed signal I/O, software driver, and hardware validation platforms.

## **Introduction**

Significant investment in IP design quality is a key element in our digital and mixed-signal design management process. This includes detailed code and functional coverage analysis, functional and timing simulations and hardware emulation.

### *Deep involvement with IP standards bodies*

Arasan Chip Systems is a contributing member to many standards bodies including MIPI, SD Association and JEDEC which enables us to have a deep understanding of interface protocol, IP development challenges and industry ecosystem development. This knowledge is applied to the design of interface IPs and also to advising customers on the latest developments. This helps us in architecting IP that meets the performance goals for the technology.

Our participation allows us to work closely with customer-representatives to understand near-term and future requirements with respect to the standards roadmaps. We have been:

- An participating in USB-IF since 1996
- An active member of the SD Association since 2001
- An active contributor to MIPI since 2005
- An active member to JEDEC since 2008
- An active member of UFSA since 2012

### *Arasan IP ecosystem*

In addition to its own efforts, Arasan engages a wide variety of ecosystem partners to leverage their expertise and experience. For example, Arasan is a member of the Cadence Verification Alliance, which aims to help customers accelerate the adoption of new technologies and improve verification productivity.

We work closely with compliance working group meetings to define and implement methods for compliance testing. We participate actively in compliance and interoperability testing events

## Development Components

Arasan's quality strategy has four components: digital IP, software, hardware (FPGA platform) and analog IP.

### *Digital IP*

In-depth protocol expertise is important element in producing high quality detailed architecture/design specifications and implementing the design . Best practices, as adopted by the design community, are followed at Arasan like following the RMM guidelines for Verilog coding. Often, the design criteria checklist provided by large customers prior to licensing the IP forms an effective cross check. A bigger component is the development of the test bench and test plans. Both Verilog and UVM/OVM based test benches are developed depending on the complexity and intent of the test bench. The main verification objectives are code coverage and functional verification across multiple segments covering protocol specification, system bus, PHY interfaces, and internal interfaces such as FIFO and sub modules. Test plans are implemented during verification phase. A number of incremental checks (e.g. Lint, CDC, LEC, STA , etc.) are performed at each step of the flow. The tool flow scripts and documentation form the substance of the IP deliverables.

### *Software*

Most complex standards-based IP today require software development that includes drivers, stacks, file systems, and application interfaces. Arasan uses a Linux platform for software development and detailed test plans are implemented as part of the qualification process.

### *FPGA Platform*

FPGAs are used to implement digital IP. The synthesized digital IP along with FPGA resources such as GTX/GTP transceivers and PCIe hard macros, and PHY daughter cards are used in a hardware platform to create a validation sub-system. This hardware validation platform, running Linux and relevant drivers, is used for full validation of a complex IP.

## IP Verification Process

Key elements of Arasan's verification strategy are Directed and Random tests, CDC Analysis and Hardware Validation.

### ***Random Tests***

Random test include Functional coverage, system black box scenarios, and internal white box assertions. A random test bench is typically designed using OVM/UVM, and implements both bus functional models (BFM) developed by Arasan and UVM/OVM compliant 3<sup>rd</sup> party Verification IP (VIP) The UVM Verification environment randomizes several combinations of parameters covering:

- System bus parameters such as bus widths, clock frequency, latencies
- PHY layer parameters, power modes, data transfer rates and error handling
- Controller specific parameters such as programming model, FIFO configurations
- I/O Protocol specific parameters such as operating modes, packet types and sizes, flow control, compliance checks, etc.

### ***Directed Tests***

Directed tests are typically used to complement code coverage scenarios, SoC Integration Suite, PHY Integration tests and specific tests for internal modules. Where required, a Verilog Test Bench is used in addition to the UVM/OVM test bench.

### ***CDC / Post-synthesis Analysis***

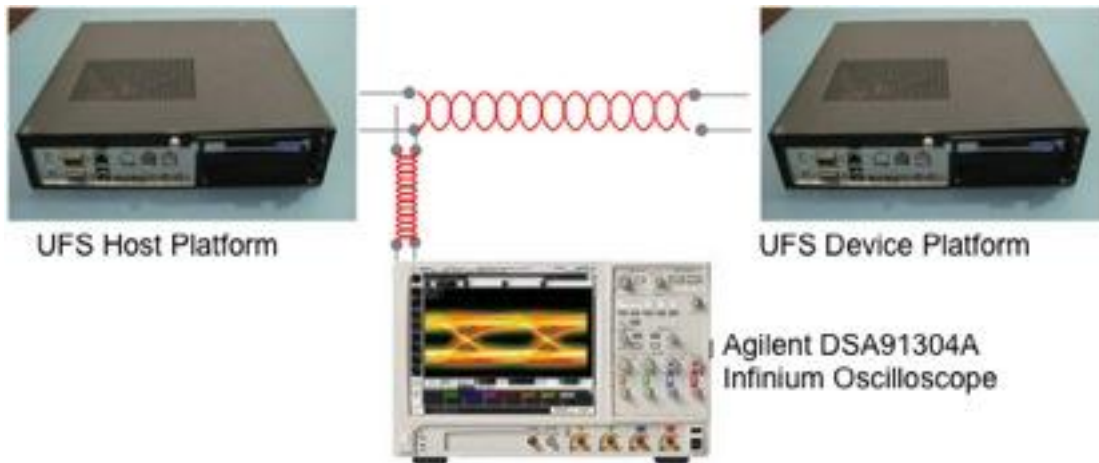
- CDC (Clock Domain Crossing) synchronization is typically implemented in one module. This simplifies the CDC analysis and generation of waiver files for tool flows. In addition it allows a generic synchronizer module to be replaced with a target library version.
- Delay-based simulation emulates synchronizer sampling delays.
- CDC signals are checked for synchronization and re-convergence
- SDF simulations to verify timing and functionality. For hard macros a wide suite of tests covering different corners are implemented. For Soft IP gate level simulations (GLS) is typically run with unit delay.

- Power Estimation is done in line with the power management features of an IP such as Hibern8 feature in M-PHY.
- Scan and ATPG are done for hard macros. For soft IP also these are verified to make sure that IP is scan friendly.

*Hardware Validation Platform*

Arasan develops and markets FPGA based platforms configured for a number of digital and analog IP products. Customers and eco-system partners use the HVPs as:

- A platform for early software development
- A platform for SoC validation
- A platform for production testing
- A platform for compliance and interoperability testing.



**Figure 1. Arasan's Hardware Validation Platform with Agilent Scope**

The Arasan HVP provides multiple use models depending on the target IP and application. The UFS-HVP can emulate the host to validate the customer's end device or emulate the device, to facilitate software debug on the host side. When paired together as shown in Figure 2, the interoperability of the complete path from host to device over the M-PHY interface can be monitored including packet transmission and signal BER quality.

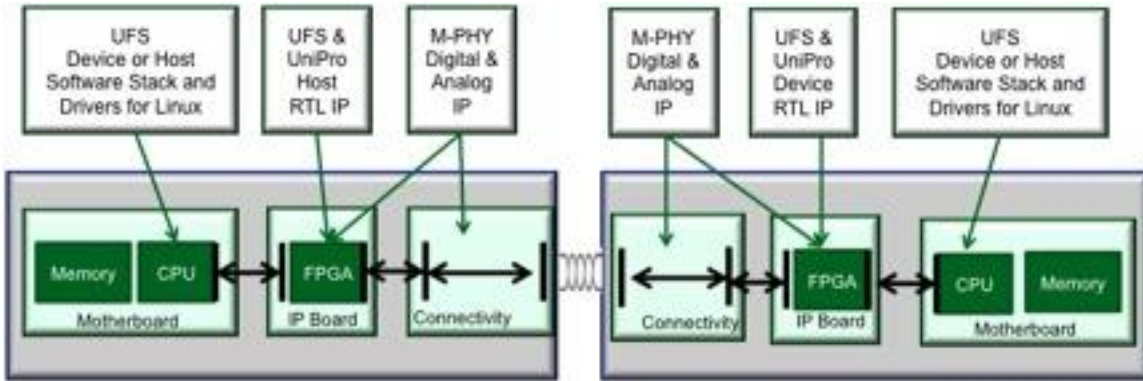


Figure 2. HVP Configuration for UFS (host) to UFS (device) Validation

**Digital Design Flow**

Tool Name	Reports	
VCS	Sim logs, toggle code coverage	
Incisive	Sim logs, toggle code coverage	
Model Sim	Sim logs, toggle code coverage	
Design Compiler	Timing & Area	
RTL Compiler	Timing & Area	
0-In	CDC warnings/errors	
Sypglass	CDC warnings/errors	
	Lint & DFT	
Conformal	LEC	
Prime Time	Static timing	
	Estimated power	
Fastscan	ATPF fault coverage	
Xilinx ISE	Area & Timing	
		Synthesis
		Gate Level Sim
		CDC Analysis
		STA
		Power Analysis
		DFT/ATPG
		FPGA

Table 1. Digital Design Flow

## **Analog IP Verification**

### **Bus Functional Model M-PHY BFM**

- The BFM is used for verification of the controller and the digital front end (DFE) of the PHY during development.
- Generated from the analog schematics
- Used for functional sign-off verification
- Exercises all the control and data path between the AFE and DFE

### **Top schematic Model M-PHY.Top**

- Models the actual implementation in the PHY.
- Dfetop.v – digital control logic (RTL or synthesized netlist)
- Afetop.v – analog front end

### **Analog Test Environment – M-PHY**

Standalone test environment verified with 3<sup>rd</sup> Party VIP. Provides a comprehensive suite of random and directed tests. Exercises all modes and configurations. Includes SDF back-annotated gate level simulations

### **M-PHY Test Cases:**

- H/W reset test (reset M-PHY attributes), Attribute Read / Write test
- LS-Burst, HS-Burst
- Reconfiguration Test Random speed / gear reconfiguration
- Error Injection tests (HS / LS burst with symbol errors)

Analog IP is delivered as GDS and is created and validated to ensure compliance with SoC design flows in the target foundry process. Deliverables consist of:

- Compliance matrix results
- User guide
- Layout integration guide
- DRC, LVS, ERC reports

### Mixed Signal Verification with M-PHY

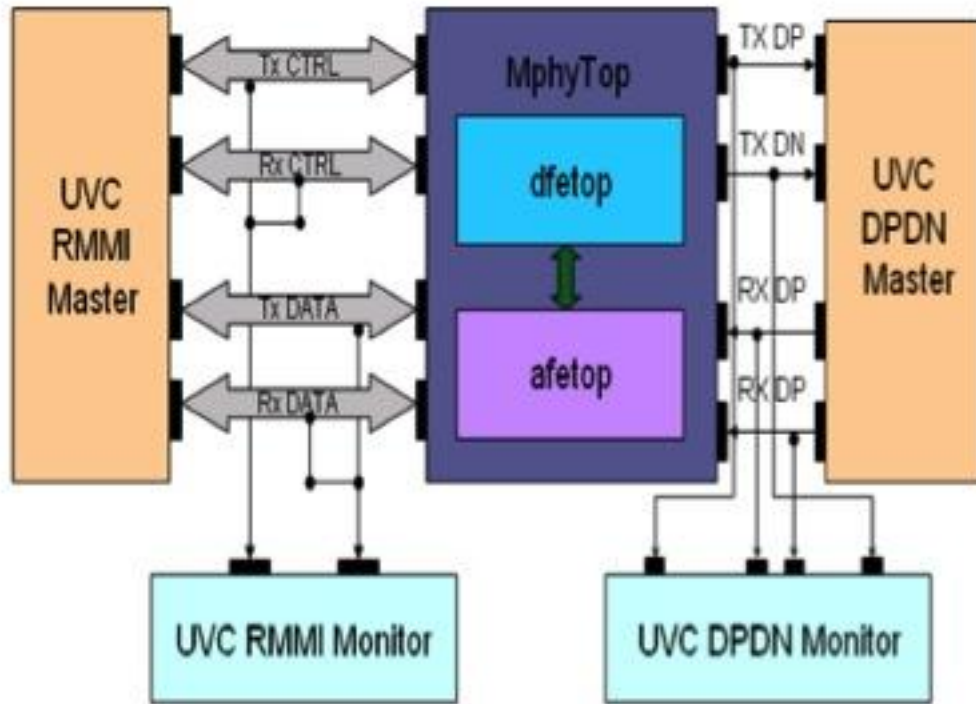


Figure 3. UVC Test Environment for M-PHY



## Analog Design Flow

Steps	Comments
SOW	Review Statement of Work for completeness
PDK Sign-off	Trial Flow with PDK Trial synthesis with .LIB Trial Pad Ring with I/Os
IP Spec	Top Level Blocks SOW Customization
Schematic	Port Schematics to PDK Anticipatory Layout Parasitics Anticipatory timing at the Analog-Digital interface Process Corner Simulations (PVT) Add trim functionality Preliminary Design Review
Layout	Understand Foundry Rule Constraints Block Layout with existing templates and best practices, e.g. high speed signal shielding
Place and Route (digital)	I/O Placement on floorplan 2X clock spacing, low power and low skew clock trees, SCANDef, Timing Signoff with OCV and crosstalk checks.
Analog Verification	Extract block level, simulate worst case corners, Top Level TTT,SSS, FFF simulation ScanDEF for scan reordering
Compliance Matrix Review	Compare to Spec
Quality Assurance	Verify GDS stream-in. all errors verified or waived GDS passes LVS, DRC antenna & extraction All waivers documented and explained IP instantiated in a top-level netlist verified in PnR environment LEF is verified to ensure pin locations & connectivity matches Integration Guide Timing Analysis with .LIB verified with sign-off timing at the interface pins

Table 2. Analog Design Flow

## Summary

Our mission is to deliver high quality IP solutions with a commitment towards zero defects through continuous quality improvement.

Semiconductor IP has evolved from synthesizable RTL to full IP subsystems encompassing digital functionality with processor-specific interfaces, application-specific software stacks, device-specific software drivers and mixed-signal interface technology. And the requirements for achieving IP Design Quality continue to evolve. Our detailed verification matrix is shown in Table 3 below.

## Verification Matrix

Item/Category	System Bus Spec	Protocol Spec (IP interface)	Programming Model Spec	Module/Interface Spec	Compliance Suite	Test Bench/ Mode
Directed Tests (All Configs)	SoC Integration	Focused Spec Items	Focused Host/Device Operation	Focused Module Link/Fifo...tests	Compliance suite where applicable	Internal BFM and Verilog/SV DVE (Design Verification Environment)
Random Tests (All Configs)	Randomize system parameters	Randomize I/O spec parameters	Randomize Master/Slave and operational parameters	Check internal interfaces with Assertions	Compliance suite - Complement Directed tests	3 <sup>rd</sup> Party VIP and ACS BFM OVM/UVM Methodology
H/W Validation	Application (e.g. SCSI CMDS) S/W Driver Host/Device stacks	Spec Items supported by H/W Config	Focused Host/Device Operation	Internal FIFO interfaces	Compliance suite where applicable	H/W platform Specific
Controller-Phy Interop Tests	Spec Defined	Spec Items supported by H/W Config	Spec Defined	Phy-Link Interface	Compliance suite where applicable	H/W platform Specific

Table 3. Arasan Chip Systems Verification Matrix