Mobile Imaging and Display
with Arasan MIPI Products

Executive Summary

This whitepaper describes practical considerations and best practices for Mobile Imaging and Display for Smartphone and Tablet Computing applications as well as exploring Silicon IP selection and successful adoption based on Arasan's experience with customer engagements.

The MIPI® Alliance, which is a standards setting body jointly formed and staffed by 240+ contributing member companies from the mobile platform, semiconductor and IP industries. Arasan has been a contributing member since 2004.

This paper will review the MIPI standards for mobile devices, and cover basics of the PHY-Controller interaction and why it is advisable to source both IP's from the same vendor. Next we provide detailed view of the MIPI D-PHY for use with various imaging applications and advanced process nodes, like 28 nm. This paper also explores various applications and connectivity with cameras and displays, and defines the practical considerations for selecting and using CSI-2, DSI and D-PHY IP's.

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Introduction

This whitepaper describes practical considerations and best practices for Mobile Imaging and Display for Smartphone and Tablet Computing applications and explores Silicon IP selection and successful adoption based on Arasan extensive customer engagements over the past three years.

MIPI Standards and Arasan IP

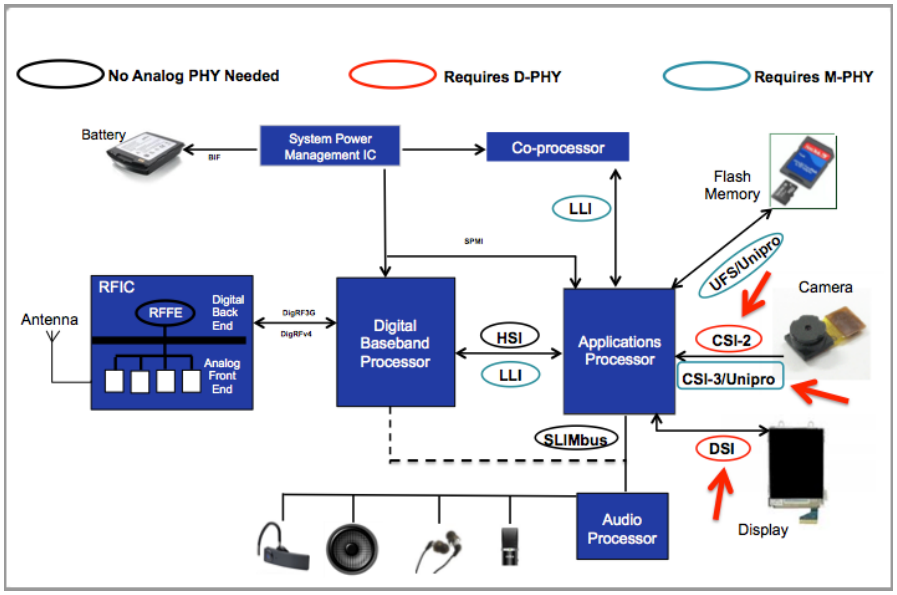

Figure 1. The MIPI Alliance set of standards

The MIPI Alliance, is a standards setting body with over 240 contributing member companies from the mobile platform, semiconductor and IP industries. Arasan has been a contributing member since 2004, and has been an active participant in several working groups, including the PHY working group. This provides Arasan with a deep understanding of the standard and protocols, and more importantly the context in which the IP's are intended to be used in the end products. Figure 1 depicts the major components in a typical mobile platform. This whitepaper focuses on the connectivity to cameras with CSI-2, to displays with DSI, and on D-PHY, the physical layer for both of these link layer protocols. Arasan IP's for all the protocols or named standards shown as circled are available including the latest CSI-3 standard.

CSI-2 and DSI standards have been around for many years, however, it is only in the last three years, particularly in the last 18 months, when we have seen rapidly increasing adoption in the mobile device industry. As mentioned before, both these standards assume D-PHY as the physical layer. D-PHY allows power efficient, EMI reduced, serial communication between a CSI-2 or DSI host/device pair. All three standards have been updated and revised a number of times. There are other MIPI standards, like SLIMbus, that do not require an analog PHY, while all the new protocols, like LLI and CSI-3 require an M-PHY as the physical layer. Not only that, CSI-3 also uses Unipro^{SM} as the link layer. Hence CSI-3 is not backward compatible with CSI-2. Arasan tracks the evolution of these standards closely. Arasan provides complete MIPI IP solutions for all these standards.

Controller + PHY – Why a combination solution is needed

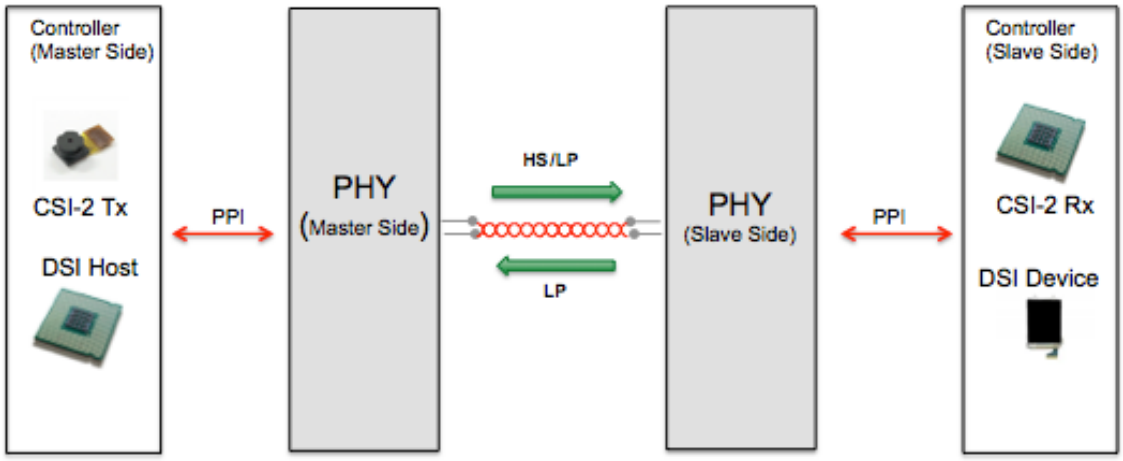

Figure 2. Controller + PHY Configuration

Designers all look for the most affordable best in class solutions. Often, the method employed is to select two different solution subsets from two different vendors. To understand how well such an approach would work, let us first examine how a D-PHY and a link protocol controller, like CSI-2 or DSI, are supposed to work together. When looking at connectivity between and host and device, or a transmitter and receiver, there is a controller on the master side that is generally responsible for configuration and control, and in this case, the source of image data. The slave controller is the consumer of image data. Each side has its own D-PHY, which communicates with the

other DPHY through a pair of wires which operate with differential signaling when transporting image data at high speed, and with single ended signaling when communicating control and status information at low speed. In MIPI parlance, serial high-speed transfers are done in HS mode, while low speed (or low power) transfers are done in LP mode. When no data is to be transferred by either side, the D-PHY's enter a deep power saving mode, called ULPS, which stands for Ultra-Low Power State. When the two sides resume communication, they transition from ULPS to LP state, then move to HS mode in case high-speed transfers are needed. The transition is initiated by the master side controller. The slave side D-PHY and the controller react accordingly. This makes the D-PHY/controller interaction much more power efficient, and takes it well beyond the capabilities of conventional SerDes based approaches.

PPI Interface

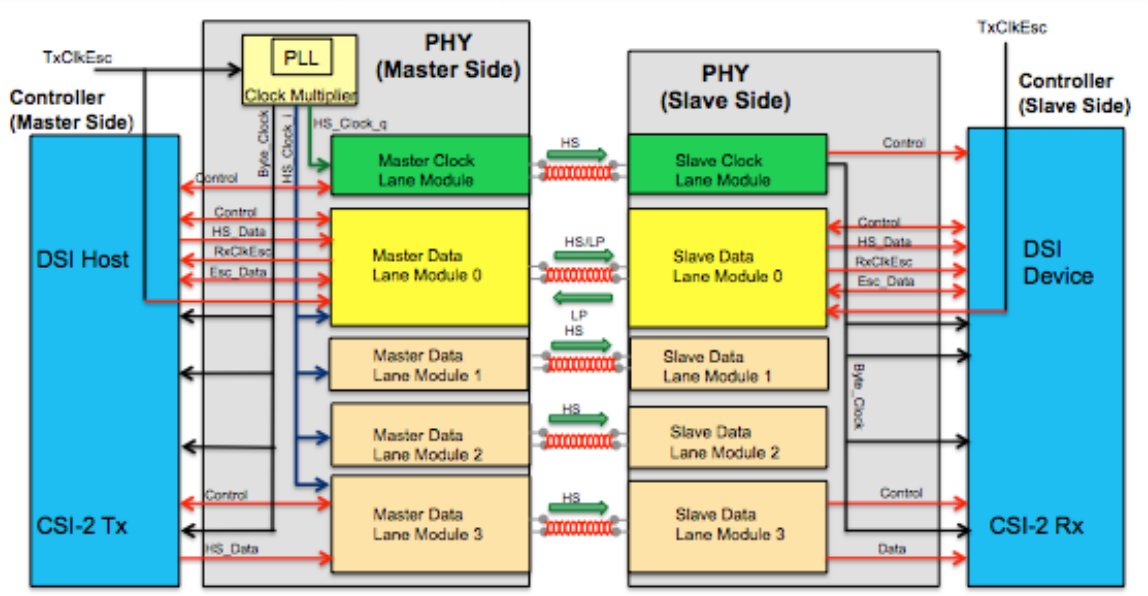

Figure 3. Detailed PPI Interface between host and device

The interface between the controller and D-PHY is called the PPI Interface. When a MIPI compliant camera needs to communicate with a compatible receiver in a mobile apps processor, all data transfers are done from the CSI-2 transmitter on the master side to the receiver in the slave side in high-speed mode. LP mode is used only as an intermediate state to transition between ULPS and HS states, and is not used for transfer of control or

status information in either direction. Hence only a subset of the signals defined for the PPI interface is needed for MIPI camera connectivity.

In the case of DSI the source of image data is the Apps Processor IC, hence the DSI Host is the controller on the master side. Either the DSI Host or Device can send control and/or status information, hence the nature of LP traffic is bidirectional. HS traffic remains unidirectional, that is, from the DSI host to the device resident in the display panel module. In this case, the full PPI interface is used.

For CSI-2 and DSI, MIPI defines a separate clock lane, and up to 4 data lanes connected with a differential signal pair. The maximum serial data rate for HS data transfers is 1.5 Gbps per data lane.

On the master side, a TxClkEsc (typically 15 - 20MHz) is used as a reference for the PLL to generate three clocks. One is a byte-clock, which is always an eighth the output data rate (1/4th the speed of the HS clock), and is used to transfer parallel data from the PHY in the master side to the slave side. The second is the HS_clk_i, which is used to clock serial data from the data lane modules. The third is the HS_clk_q, which is quadrature phase shifted with respect to the HS-clk_i. The quadrature shifted clock is converted to a differential form in the master clock lane module, and shipped over the differential signal pair to the slave clock lane module which, in turn, converts and divides down to the byte-clk for the slave side. The quadrature shifting ensures that HS data arriving in the slave data lane modules is latched properly.

All data lanes can transfer data in HS mode, while only Data Lane 0 is capable of transferring data in both HS and LP mode. In Ultra-Low Power State, there is no data transfer, and the high-speed transceivers in all the data lanes are turned off. However, during LP mode transfers, the TxClkEsc is used to generate the data, while the receiver on the other side recovers the clock from the data stream. Remember, LP transactions can be driven from either side.

Either side may attempt an LP transfer at any time. The direction of data flow may be the same or the opposite of an existing high-speed transfer. This would require the differential bus to turn around, and be able to do that

without premature LP transfers causing bus contention. Also, if a bus contention does occur, the system has to recover from it by stopping the transfer and allowing the controller on the driving side to retransmit.

All these factors need to be taken into account when designing a D-PHY, which led to Arasan's development of a universal version that can work with both CSI-2 and DSI protocols.

MIPI D-PHY – design for today's needs

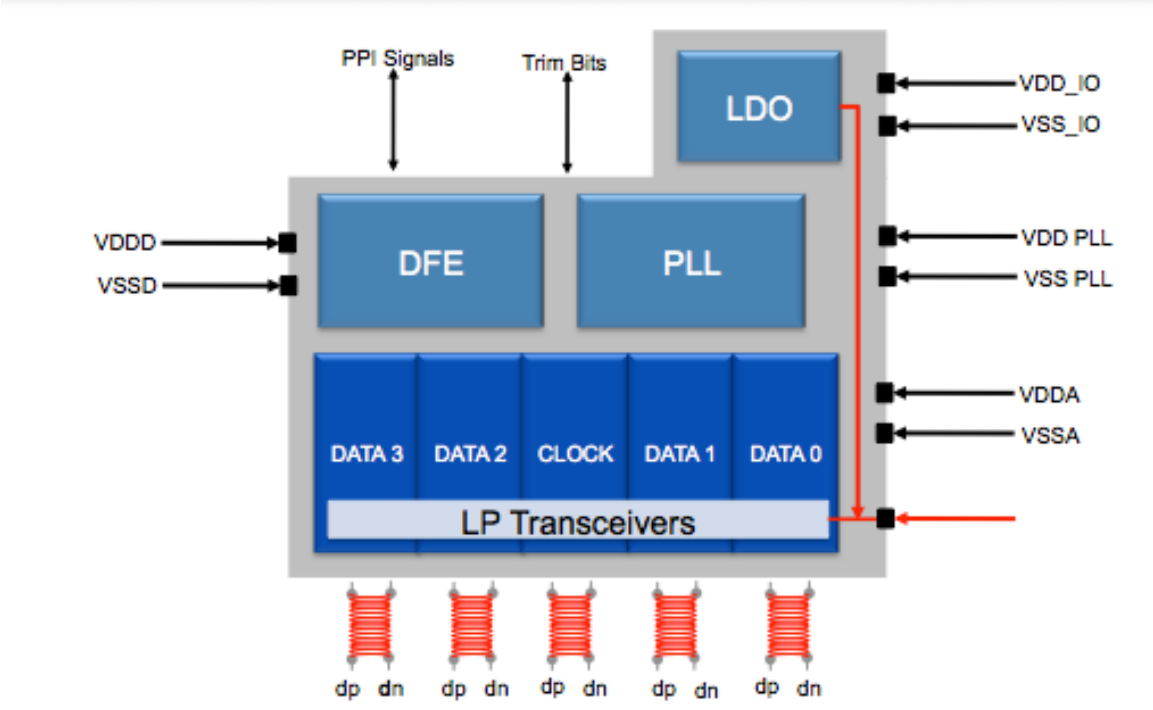

Figure 4. MIPI D-PHY

The Arasan D-PHY is split into three main sections. The analog front end contains the PLL and clock lane module, and for each data lane, the transmitter and receiver that can drive and receive both HS and LP data on the Dp/Dn lines. There is a separate contention detection module that reports contentions on the Dp/Dn lines during bus turnaround. This block is disabled for CSI-2 applications.

The second section is the digital front end, which contains the data serdes, and is responsible for correct data sequencing when multiple lanes are

active. In Arasan's universal D-PHY design, Analog BIST is included which allows production testing of the AFE using internal loopback from transmit to receive data paths. During The mux/demux structure allows the D-PHY to be used in either normal operation or BIST mode.

Analog BIST requires the presence of both the transmitter and receiver, hence although only one of them is needed in a CSI-2 application. We provide D-PHY IP with both present to allow production testing.

In summary, Arasan's universal D-PHY design is usable for both CSI-2 and DSI protocols. When licensing a D-PHY, the designer needs to specify the number of lanes. Arasan can deliver IP with the number of data lanes required, and each data lane comes with analog BIST as well as both the transmitter and receiver blocks. There is also a choice of IO pad topology: staggered, in-line or flip-chip,

Hence, when selecting an IP vendor for D-PHY, designers need to understand their willingness and capability to either configure or modify their D-PHY to meet specific needs. The mere claim or availability of a D-PHY test chip is not sufficient. The test chip may not be in the silicon process you have committed to for your project, and the pad routing and lane configuration may not match what you need. Arasan excels at making the proverbial shoe fit the foot, not the other way around.

Advanced process nodes present special challenges. The MIPI spec requires the LP transceivers to operate at 1.2V. During LP transfers, the Dp/Dn lines of the differential pair have single ended CMOS level signaling. Hence if the core supply voltage is 0.9V, the spec will not compliant for LP mode. Arasan's D-PHY provides an extra power pin for a dedicated 1.2 volt supply to be provided from an external source on the PCB. The second option is to use an Arasan-supplied LDO that steps down a 1.8/2.5/3.3V external supply to the nominal 1.2V required by the specification. This alternative comes with a small area overhead.

Display Connectivity with DSI

The MIPI DSI standard allows interface to four types of display panel modules. These panels differ in whether their display driver logic is able to buffer full or partial frames, how programmable they are, and to what level they are able to send and receive display commands or requests to and from the host processor. Type 4 panels have the minimum capabilities, and every display frame has to be explicitly sent from the DSI device. Data flow from DSI host to device is always unidirectional. Image data transfers are made between the DSI device and the Type 4 display drivers within panel modules over the DPI interface, which is also specified by MIPI. At the other end of the panel spectrum is the Type 1, which is able to advertise to the host its capabilities. This is done by the panel's display driver logic sending LP transactions to the host processor. Hence, LP data flow is bidirectional, while high speed transfers are always from the host processor to the display panel module. Such transfer characteristics are defined in MIPI's DBI specification, and the control and command sets are defined in the DCS specification.

Type 2 and 3 panels can support both DPI and DBI transfers. They have partial or no frame buffer memory, and when operating with DPI transfers, rely on configuration information stored in their non-volatile memories. In general DBI transfers are a lot more power efficient, since an explicit transmission does not have to happen for every refresh of every frame.

Mobile displays, particularly tablets, have been trending towards increasing resolution and color depth. MIPI, in anticipation of this, has defined the DSI and D-PHY connectivity standards to allow plenty of headroom. With 4 lanes of 1.5Gbps D-PHY's, designs can go up to 2.5Kx2K resolution, which is beyond the most advanced tablets available in the market today.

Camera Connectivity with CSI-2

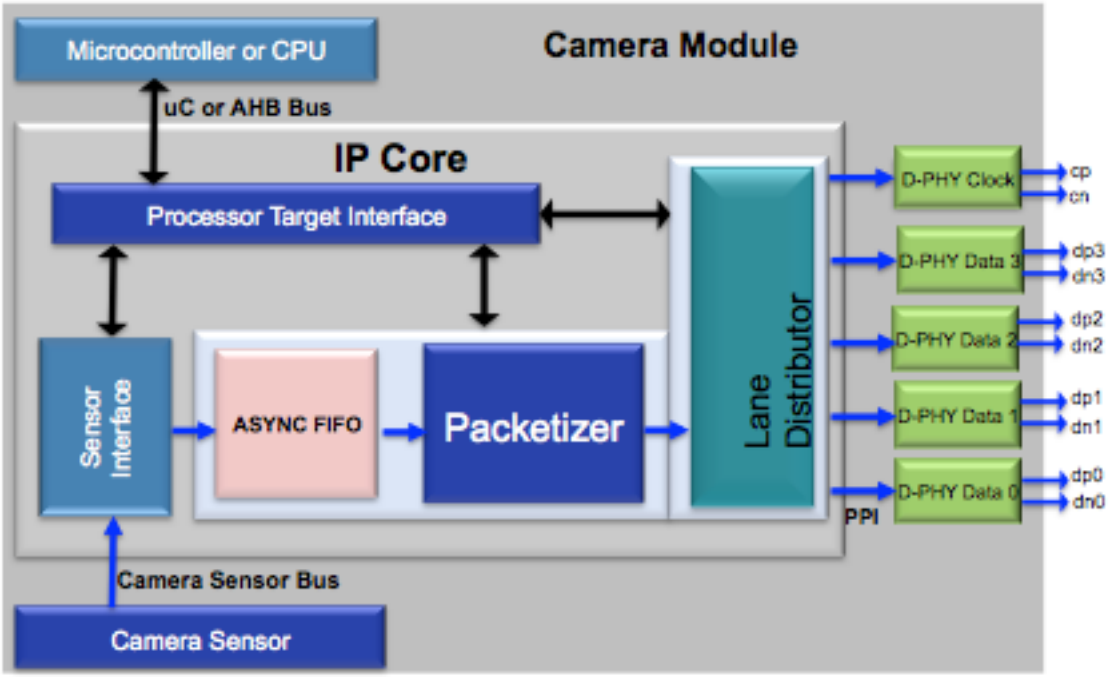

Figure 5. CSI-2 transmitter

For the purpose of this discussion, a camera module consists of an image sensor, a microcontroller or CPU subsystem, and the CSI-2 transmitter IP with its associated D-PHY. Image data captured by the camera sensor should be presented to the CSI-2 Transmitter in RAW, RGB or YUV formats; the MIPI spec lists all the detailed formats that the CSI-2 connectivity infrastructure is required to support. The CSI-2 sensor interface provides you the option to compress the RAW data, and converts any kind of pixel data to bytes, which are then packetized and distributed over one or more lanes of the D-PHY. The higher the resolution of the captured image, the more speed and/or number of lanes needed. Given the max D-PHY throughput of 1.5Gbps per lane, with a maximum of 4 data lanes, the maximum camera resolution supported, assuming 24 bits/pixel in RGB format, with 30 frames/second is 8 megapixels.

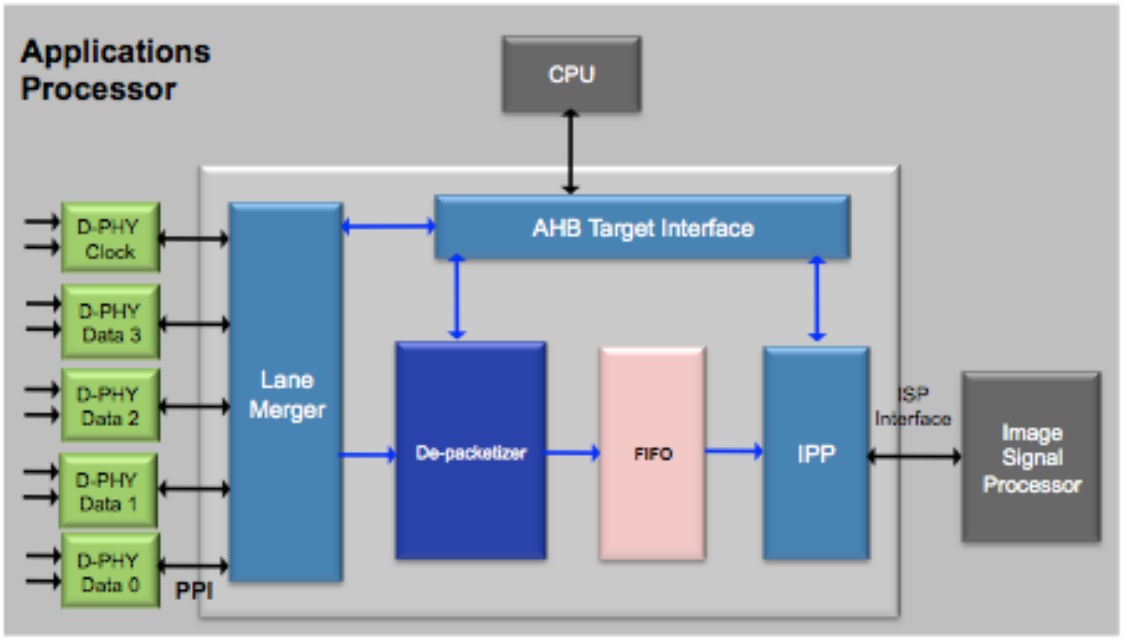

Figure 6. CSI-2 receiver

The CSI-2 receiver resides in an apps processor. The original camera image sensor data split into multiple lanes is grabbed from the slave D-PHY's and merged. The depacketizer checks for CRC errors in the payload, before forwarding the image data to the ISP interface. The FIFO is used to pass data from the depacketizer's byte clock domain to the ISP clock domain. This receiver has the flexibility to transfer one or two pixels per ISP clock. The ISP interface block frames the image with the appropriate front and back porches for the horizontal and vertical blanking periods.

Configuration, control and status reporting is done using programmed IO through the AHB interface. Both the CSI-2 receiver and transmitter are configurable for any allowed number of lanes. However, Arasan remain flexible in customization, since our objective is to ensure proper integration of this IP into the rest of the SoC.

A typical mobile platform has front and rear cameras, and there are choices to be made with respect to the bit rates to be supported for each camera subsystem. The choice of the camera sensor governs the number of bits per pixel and the size of the pixel row/column matrix. Different customers target different resolutions, color depth and frame rate, and that determines the

lane configuration and maximum high speed data rate for high speed transfers.

To illustrate these choices, consider the design team that decided to offer the option of either a single rear camera, or dual stereoscopic rear cameras. To stay within a target power budget the options offered here are to either provide the maximum resolution and color depth with a single 4-lane rear camera, or reduce the resolution and color depth when operating in stereoscopic mode with two 2-lane cameras. In stereoscopic mode, two of the lanes in CSI-2Rx_0 are shut down. Other customers may choose other configurations, and this lends itself to customization in the ISP interface – an example being the transfer of 2 pixels per ISP clock. Arasan is able to collaborate on this kind of architecture planning and customized implementation. MIPI standards mostly deal with data transformations and transfer protocols, however, close cooperation between IP vendor and user is required for integration. This has major implications for the verification IP that Arasan delivers with each IP, since each customized feature has to be verified through simulation and coverage analysis.

Looking Forward to CSI-3

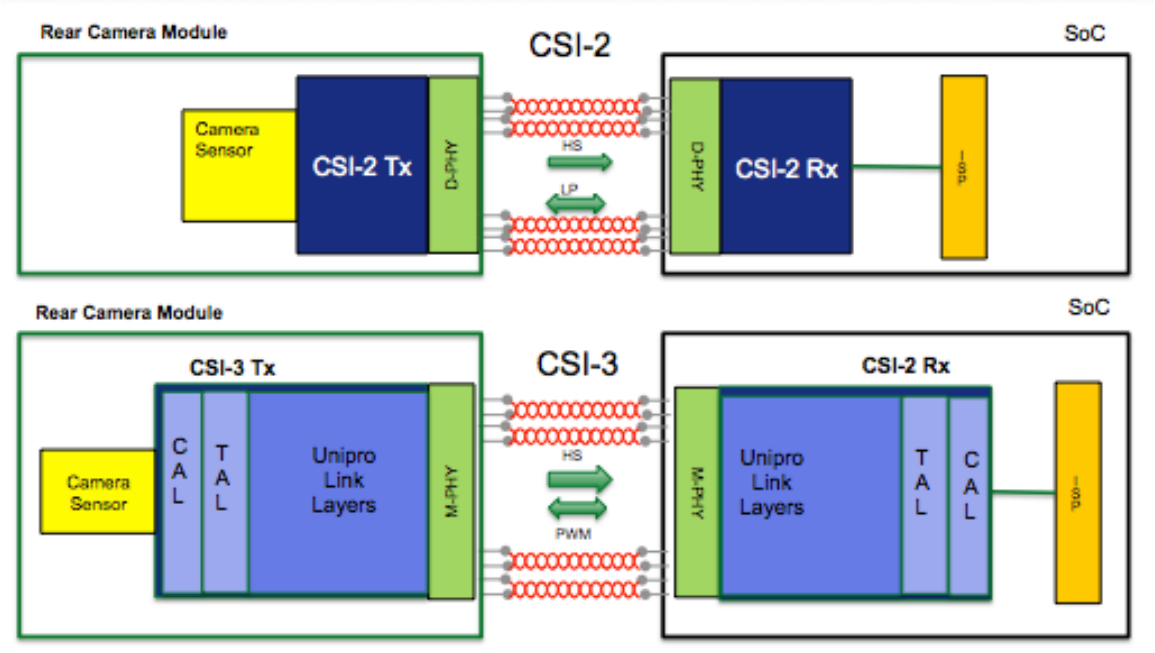

Figure 7. CSI2 and CSI-3 Differences

The CSI-3 Rev 1.0 spec was released in February 2013. CSI-3 uses M-PHY for the physical layer. M-PHY is quite different from D-PHY. It does not have a dedicated clock lane, and relies on clock and data recovery on the receiver side. Two different speed gears are supported for high-speed transfers, namely, 1.5 and 2.9 Gbps, also with a maximum of 4 lanes. The LP mode transfer is replaced with a PWM mode transfer, which is also differential in nature, and has support for multiple clock gears. This means that a camera and SoC will need to auto-negotiate the maximum speed that they can run at – both for HS and PWM modes.

The controllers use the MIPI Unipro protocol for its link layer. This, along with M-PHY, has been designed, verified and deployed in live customer engagements for other applications by Arasan. What is new, and strictly speaking, defines CSI-3 are the transport and camera abstraction layers above the Unipro. These specs are under review at MIPI.

From the physical to the sensor or ISP interface, CSI-2 and CSI-3 are different at every level, so backward compatibility using the same Dp/Dn lines is not possible. One may choose to provide both options on an Apps Processor SoC by integrating two different sets of IP's driving two different sets of Dp/Dn lines. CSI-3 adoption will be driven by mono and stereoscopic cameras that support resolutions, color depths and frame rates beyond what is possible with CSI-2.

Practical Considerations

In summary, if you are considering selecting MIPI IP for mobile imaging, Arasan strongly recommends that you license the PHY and Controller from the same vendor. The PPI interface and some low level details can be implemented with both IP's in mind, and it is not recommended that you spend time on compatibility issues between two different IP's during a live project. The D-PHY is a sophisticated PHY, and successful adoption requires the IP vendor to deliver low power, small area, testability, spec compatibility at sub-40 nm, and configurability to match your packaging, process and application. For controllers, every target chip design seems to require some level of architectural flexibility or customization in the IP. Arasan is committed to serve an expansive market for cameras and displays, including dual and stereoscopic imaging and different host bus interfaces. Additionally, new cameras and display panels continuously evolve, and ensuring compatibility between SoC's and such peripherals frequently requires intervention by IP vendors. To this end, Arasan recommends that Application Processor designers source samples of the camera or display modules and interface them to Arasan's hardware validation platforms to enable early hardware software validation.