

Full Speed Validation Platform for Mobile IP

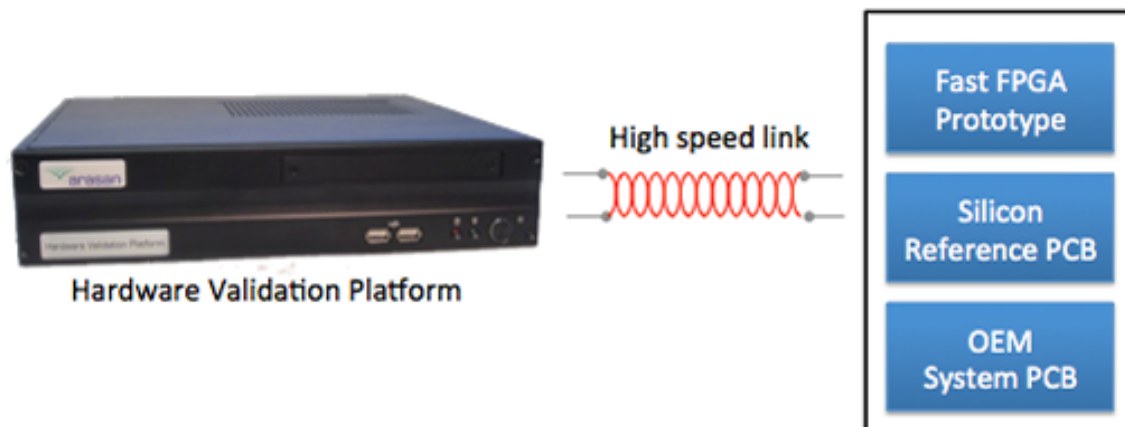
By Andrew Haines, World Wide VP Marketing

Executive Summary

Mobile systems rely on a large number of complex IP functions for memory and peripherals subsystems.

To enable rapid adoption of digital IP into customer silicon, most design IP vendors offer synthesizable RTL source, synthesis scripts, and verification IP. For analog and mixed-signal IP, most vendors offer a complete physical design package, along with chip integration guidelines. These deliverables address design integration and functional verification, however, for evolving standards there are other gaps that early adopters must fill to realize the competitive advantage of right-the-first-time development with the shortest time to market.

Emulation has become a critical component of system design, allowing hardware and software development and debug to proceed in parallel. For peripheral subsystems, the host and it's associated application stack communicate with a device and driver. And increasingly a high-speed serial link is involved. This is the point where emulation must be complemented with hardware validation.



Mobile Connectivity Standards from the MIPI Alliance®

There is an ever-increasing choice of mobile storage and connectivity silicon IP for camera, display, low-speed e.g. audio, Bluetooth, etc. available in RTL or GDS-II form. For mobile connectivity, the largest growth is seen with MIPI protocols. The MIPI standards organization has and actively continues to define and drive a spectrum of optimized standards for interfacing among application processors, baseband and RF IC's, human-machine interfaces, power management controllers and RF front-end components. According to sources quoted by MIPI, the number of MIPI-powered IC's will grow to 6.2 billion units by 2015, with at least one MIPI specification reaching 100% of smartphones by 2013.

IC to IC Connectivity

Each connectivity or storage standard defines the protocols and signaling requirements for two or more devices to communicate with each other. Any device (like a mobile applications processor) requires a complementary device it communicates with (like a display or camera module) that adheres to the same protocol and signaling requirements. The two complementary devices either operate as peers, or as a master and a slave.

High speed serial I/O & link layers

To increase battery life and minimize chip pins to reduce package, serial interfacing is becoming increasingly popular. In the recent years, the complexity of these standard protocols has ballooned, with the introduction of serial interfaces and multi-layered links, like those based on MIPI UniproSM need to identify and enumerate other devices, configure themselves accordingly, and manage the data transfers according to the capabilities of other devices and the requirements of end-user applications.

The Silicon Validation Gap

A silicon vendor introducing a new storage or mobile connectivity interface will ultimately need to validate his device, usually implemented as an FPGA prototype, with a complementary device. Often, a silicon vendor who is an early adopter of a standard, may not find complementary devices ready for validation soon enough. That raises the need for cost-effective, protocol and signaling-compliant, full speed alternate solution for a complementary device.

Validation vs. Emulation

Traditionally, for connectivity protocols like USB, PCI-Xpress, etc. the semiconductor community has used hardware emulation for design validation purposes. Since those systems also incorporate major portions of the complete chip design, partitioning across multiple FPGA's or specialized processors impose upper limits on performance. Speed matching solutions or "slow down" solutions allow interfacing to external hardware like testers, which run at their native speeds. A number of interfaces, like those from MIPI, present new validation challenges. Speed matching solutions for those protocols do not exist, and PHY's are out of the scope of those solutions in any case. Moreover, the high cost of those solutions prevents scaling to downstream use models like production testing. What is needed is a set of platforms that allow standards compatible, at-speed execution of new connectivity protocols, with the appropriate hooks for software/driver development, ultimately leading to a cost-effective production testing infrastructure.

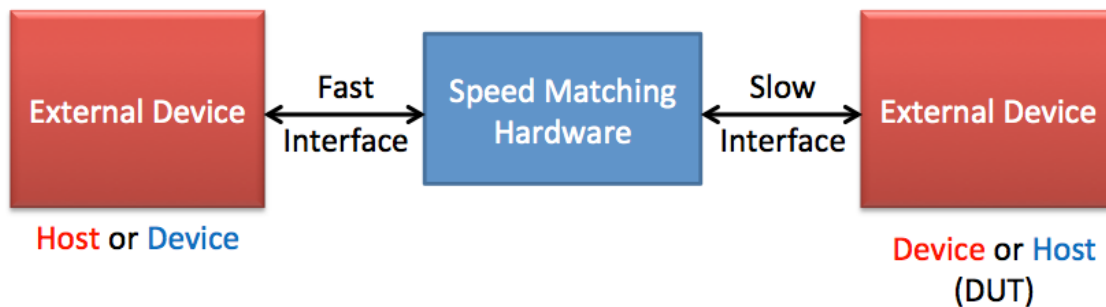


Figure 2. Limitations of Emulation

Arasan Hardware Validation Platform Detail

Arasan's [family of Hardware Validation Platforms](#) provides such a solution. They are targeted for various connectivity protocols that span imaging, camera, audio, storage and inter-chip connectivity protocols for mobile platforms. These platforms are not meant to replace traditional emulators, but to complement them.

Each connectivity protocol has two sides to a connection – a host or master, and a device or slave. The protocol standards specify the schemes for data and control encapsulation before being sent over a physical medium, and payload extraction when received from the same medium. These schemes are

implemented with connectivity IP's which themselves are programmable for different configurations and modes of operation. Many of these schemes impose timeouts and transmission retries, which mandate at-speed operation.

Arasan offers separate validation platforms to separately model host and device functionality for many of the mobile connectivity protocols. A given platform emulates a peer or target that a DUT is meant to communicate with, hence is a perfect platform for validation of the DUT when it is implemented and ready for testing within an FPGA prototype, a silicon reference board or part of a complete system. Note that the scope of the validation is limited to the configuration and runtime behavior of the specific connectivity protocol between the host and the device. Since the Arasan Hardware Validation Platforms (HVP's) are based on readily available FPGA's operating within a Linux system, they are highly cost effective. Their ability to run at the high speeds required by the various protocols make them an excellent complement to verification and validation practices using traditional emulators.

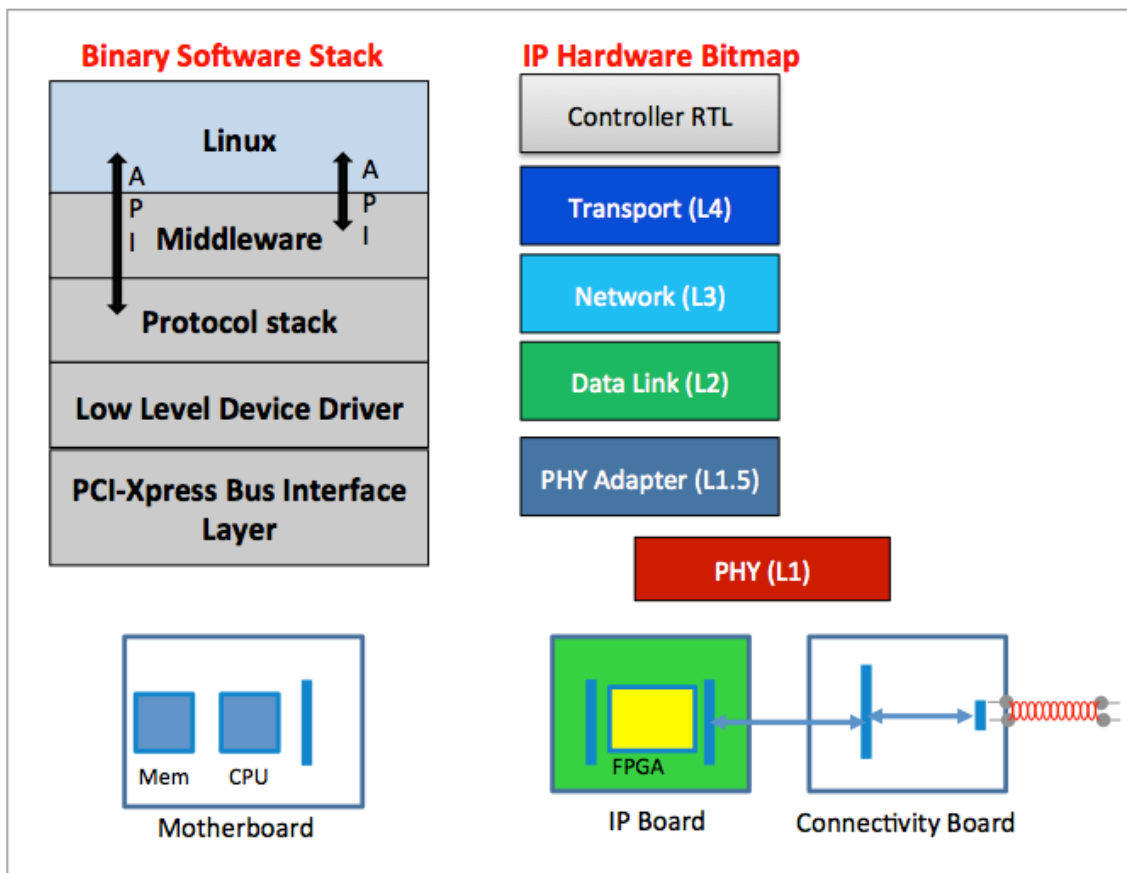


Figure 3. Inside the HVP

The hardware is comprised of a standard Linux PC platform, with PCI-Xpress connectivity to an FPGA board that contains the Arasan IP. For external interface protocols that require an analog PHY, like D-PHY, M-PHY and USB-2 PHY, there is a special connectivity board that is mounted onto the FPGA based IP board, with SMA connectors provided for easy hook up to DUT hardware environments. For each protocol there is typically a host platform and a separate device platform, which emulate the link and PHY for the host and device respectively.

Software stack binaries are included in the platform, with user-friendly interface and a rich set of debug messaging features. When interacting with the DUT, the HVP provides the runtime control (where applicable) as well as runtime execution messaging. This makes it the perfect vehicle for connectivity protocol specific validation.

The software stack has a well-documented set of API's for function driver or application development. This extends the use model from validation to software development. For this purpose, a customer typically licenses the source code for the software stack, and Arasan provides guidelines for porting to other OS's, like Android.

Such HVP use models are particularly advantageous with respect to cutting edge protocols, for which host and device capabilities do not exist in the products available in the marketplace.

Validation Starts Early in the Cycle

The validation use model applies throughout a product cycle. Consider a situation where there is a new protocol, and neither the host nor device are available in any silicon form to validate with. Your first silicon implementation of your DUT, which includes the new connectivity protocol, would typically be in the form of a FPGA prototype. You can get a significant amount of validation done with the Arasan HVP, and when commercially available products are phased in for validation, the HVP continues to serve as a golden reference to help analyze and debug any incompatibilities between the third party silicon and your DUT. The same practice can be followed with your silicon reference board, in case your silicon is available before the peer device. A number of customers have extended this use model to system validation, and have leveraged Arasan's HVP designs to create production test environments.

Validation Reduces Time to Market

The greatest advantage that HVP's bring to the table is significant reduction in time to market. In this example, we show a scenario where the host and device silicon vendors are different entities, and have widely differing product release schedules to the OEM. Consider the case where both vendors do not have access to the Arasan HVP's. In this example, the host vendor has to wait till the device vendor has an FPGA prototype ready to interoperate with. Until that validation completes certain milestones, the OEM cannot proceed with system validation.

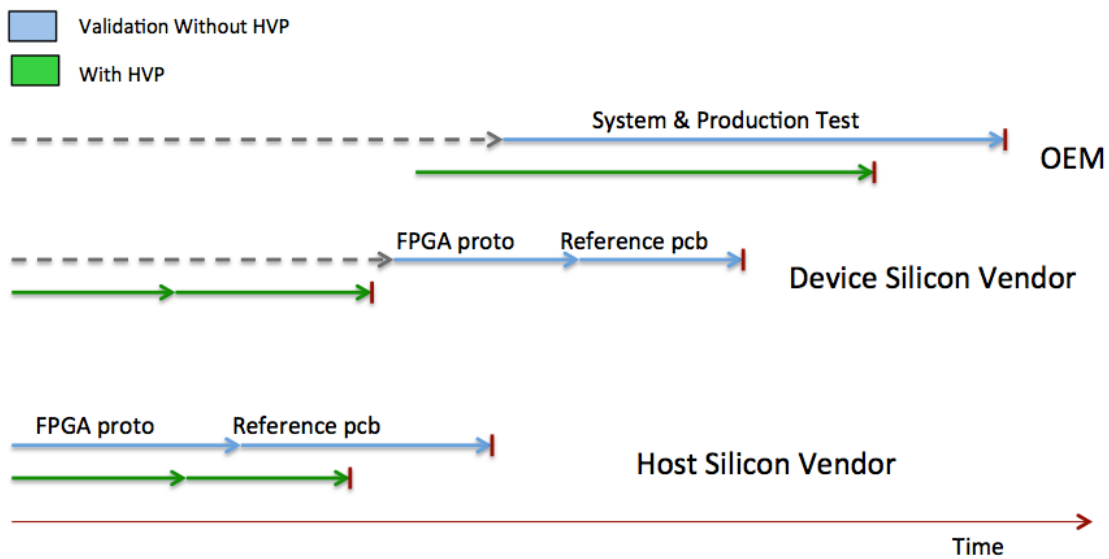


Figure 4. Hardware Validation reduces development time

Since Arasan is among the first to implement a new mobile connectivity protocol in both RTL and a validation platform, both the host and device silicon vendor can use these platforms. In this example, the host silicon vendor would get started with the Arasan HVP, then switch over to validation his prototype with the device silicon vendor's prototype. Both vendors would proceed with their interoperability and validation efforts through the end of the silicon reference board phase, and provide incremental updates to their common OEM customer. The OEM saves time to market with early validation and with platforms for early software development.

Example

Let's look at a specific example of a UFS device silicon vendor. His objective is to develop and ship a flash memory device that communicates with an apps processor on a mobile platform using the UFS protocol. This protocol uses the MIPI M-PHY as the physical layer and the MIPI Unipro as the link layer. Early flash device adopters of this protocol did not have access to AP's with UFS host capabilities, hence they chose to use the UFS Host HVP as the platform to validate their DUT's with. Licensing the UFS Device Software Stack source code, they developed their own function drivers using the API's that Arasan provides, and tested the software on a UFS Device Validation Platform before porting it to their own prototypes. In parallel, they developed a production testing application that resided on top of the UFS Host Software Stack, and leveraged the Host HVP FPGA board design to create a production test platform. All this work has been done before the first apps processor with UFS connectivity is available.

Summary

Validation of silicon and end systems with new connectivity standards is a time to market challenge. Serial connectivity with high-speed analog and differential signaling is now more of a norm with new connectivity standards. The differences lie in power management capability, bit rates, and common mode and differential voltage levels. Behind the analog PHY's are link layers that incorporate increasingly complex hardware and software protocols to increase system level connectivity options. Consequently, a true Total IP Solution has gone beyond verification and physical design enablement. Combined hardware/software modeling and implementation of target or peer devices or systems is a necessity for both hardware/software validation and software development – starting with FPGA boards, all the way through silicon reference boards and production testing. Arasan is generally among the first to implement new mobile connectivity protocols, and consequently among the pioneers who successfully complete interoperability testing sessions with other contributors to standards organizations, like JEDEC, MIPI Alliance and SD Association. Hence, among IP vendors, Arasan is generally the first to offer HVP's to fill the validation gap. That's how the Total IP Solution contributes to our customers' achieving their time to market objectives with connectivity that interoperates with peer devices correctly.