White Paper

Crystal-Less USB PHY for IoT Designs

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Arasan's Crystal Less USB PHY Implementation

Universal Serial Bus (USB) is the industry standard for enabling connectivity, communication, and power supply between computers and various electronic devices including the latest mobile Smartphones, tablets and wearables. The main reasons for USB's dominance are its ease of use, plug and play functionality and robustness. USB has simplified the way consumers control peripherals and transfer data. With over three billion USB-enabled devices shipping every year, USB is not only the fastest growing interface in consumer applications but has also achieved significant growth in industrial markets.

However, the features that make USB the preferred choice of engineers also add to their design woes, especially while designing power-sensitive, battery-operated connected device products for the Internet of Things. Adding USB interfaces to portable, battery-powered connected devices can double the application current consumption. Upgrading from a conventional serial interface for communication to the popular USB interface comes at the expense of unrealistic and often unattainable restrictions on an energy budget. Often, a developer is left to choose between doubling the battery size and increasing device cost, which makes it less appealing, or trimming the all-important differentiating features.

With the advance of IoT applications, there is an increasing demand to reduce the number of external components used. The reference clock input for USB systems are generally sourced from a crystal. With Arasan's unique ACS USB PHY IP, this need for external crystal can be removed. Arasan's offering supports a crystal-less USB operation allowing designers to eliminate the complexity of an external crystal, thereby reducing the overall cost.

ACS USB PHY uses an internal RC oscillator to generate the required reference clock for the PHY. It uses special circuits inside the PHY to limit the variation of the clock to reasonable limits upon boot up. During the reset sequence, the host transmits a SoF packet every 125us, which is used by the ACS PHY to tune the local oscillator. This tuning process is carried out in the background in such a way that before the end of the reset sequence, the local oscillator is tuned to within 500ppm of the host (as per USB specification requirements). On top of this, special monitor circuits in the PHY keep track of local variations during the normal operation and constantly tunes the oscillator. This ensures continued compliance even after the reset sequence is completed. This IP can be ported to any technology node.

Arasan's Comprehensive Library of Process Nodes

Arasan USB PHY IP is available in a wide range of process nodes from major foundries - from 180 nm to 28nm. The company has been actively expanding its lineup of process nodes to now include 40 ULP, 40 LP, 28 HPC and 28 HPM processes.

The latest addition to the lineup, TSMC's ultra-low power 40 ULP process node is geared toward the fast evolving Internet of Things (IoT) and wearable device markets that require a wide spectrum of

technologies to best serve these diverse applications. The 40ULP process supports processing speeds of upto 1.2 GHz and provides significant power reduction benefits for IoT and wearable products and a comprehensive design ecosystem to accelerate time-to-market for customers. The 40 ULP process technology not only reduces power for always-on devices, but enables the integration of radios and FLASH delivering a significant performance and efficiency gain for next-generation intelligent products.

Compared with their previous low power generations, TSMC's ultra-low power processes can further reduce operating voltages by 20% to 30% to lower both active power and standby power consumption and enable significant increases in battery life -- by 2X to 10X -- when much smaller batteries are demanded in IoT/wearable applications.

Arasan USB 2.0 PHY IP

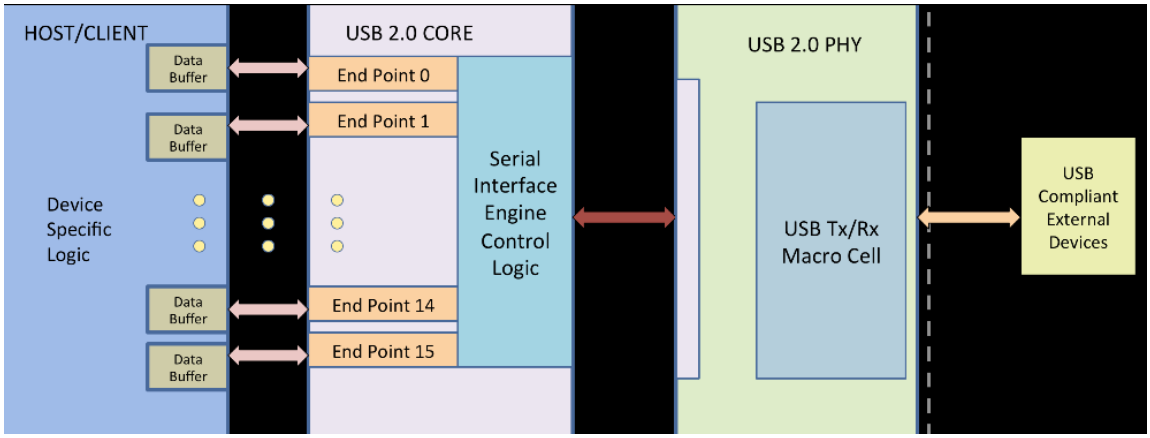
USB 2.0 PHY performs low-level protocol and signaling functions. While transmitting, the PHY serializes data, generates Synchronize (SYNC) and End-of-Packet (EOP) packet fields, and performs bit stuffing and Non-Return-to-Zero Inverted (NRZI) encoding. While receiving data, the PHY recovers incoming data and clock, de-serializes data, strips SYNC and EOP fields, and performs bit un-stuffing and NRZI decoding.

The USB 2.0 PHY is a full-featured on-chip physical transceiver. It has Electro Static Discharge (ESD) protection and fully supports all OTG and host functionality. On-board clock generation and PLL blocks provide for accurate, high-speed data transmission from and to the transceiver. When this USB PHY is used, a minimal number of external components are required.

The Arasan USB 2.0 PHY IP is a transceiver, compliant with the USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) level 3 specifications, for use with host, embedded host, On-the-Go (OTG) and function controllers. Its high speed, mixed-signal circuitry supports 480 Mb/s USB 2.0 High Speed (HS) traffic, while remaining backward compatible with USB 1.1 legacy protocol for 12Mb/s Full Speed (FS) traffic and 1.5Mb/s Low Speed (LS) traffic.

System on Chip Description

The PHY acts like a bridge between USB-compliant external device(s) and the on-chip USB core. Communications with external devices, such as host, hub or peripherals, are conveyed via the serial USB 2.0 bus, in half duplex mode. On-chip, communications between the PHY and USB 2.0 core are handled via a parallel UTMI+ bus within the PHY, selectable to 8-bit or 16-bit width. The USB 2.0 core receives data from, and transmits data to, the PHY. Per USB protocol, the core distributes data to, or receives data from, the appropriate End Point. End Points are buffers that store multiple bytes of data. The buffers are uniquely addressable. Upon power-up or detection of device attachment/removal, the USB 2.0 core, in conjunction with the host, establishes which particular device address will be allowed communication with the external USB device.



Arasan's Contribution to USB

Arasan Chip Systems provides a complete suite of USB-compliant IP including low speed, high speed and super speed USB products. Arasan became a member if the USB-IF standards body in 1996 and delivered its first USB 1.0 IP product in that year. The offering expanded to USB 2.0 products in 2000 and USB 3.0 products in 2009. Arasan's customer base includes many major systems and SoC companies in variety of industries.

Arasan is the only company to offer a USB Total IP Solution. In addition to offering a complete suite of digital IP for USB, Arasan's analog IP team onlhas also developed the USB 2.0 PHY and USB HSIC PHY. As part of its end-to-end solution approach to IP, Arasan also offers USB 3.0 software stacks and drivers which are backward compatible with 2.0 specifications.

Arasan's USB Support

Arasan has been a contributing member of MIPI since 2004. Our expertise is deeply embedded in all product offerings. Being intimately involved in developing the standards ensures that Arasan gets a head-start in understanding near-term and future standard roadmaps. This helps the company in planning product updates accordingly and in going to the market with the latest and most innovative products. Customers in turn reap the benefits of being the first mover.

Arasan's strategic partnerships in the IP ecosystem help the company in defining and implementing methods for compliance and interoperability testing. Arasan works with its customers from the onset in defining their MRD and architecting their SoC designs. The company is cognizant of its customers' specific requirements and offers IP customization services to help them achieve product differentiation.

Arasan stands by its solutions with the support network of highly skilled engineers who are directly involved in developing the code and therefore possess an intimate knowledge of the IP standard. Arasan is also one of the very few companies that offer support on customized IP in addition to standard IP.