

## Features

### SD/SDIO:

- Meets SD Host Controller specification Version 2.0 Part A2
- Meets SDIO v2.0 Specification Part E1
- Supports scatter-gather ADMA2 mode
- Supports non-DMA, SDMA, ADMA1, and ADMA2 modes
- Supports SD High Capacity (SDHC) and SD High Speed (SDHS) cards standards
- Host clock rate from 0 to 50 MHz
- Up to 7 functions in SPI, SD1, or SD4 mode
- Up to 200 Mbit/s with 4 parallel SD data lines
- Supports Test Register to generate events by software
- Hardware interrupt to host
- CRC7 and CRC16 modules
- Supports direct R/W (IO52) and extended R/W (IO53) commands
- Supports Read Wait Control, Suspend/Resume operations
- Supports multiple slots/cards
- Programmable through AMBA 2.0 AHB bus

### System Architecture

- Supports 32-bit system bus
- Host clock rate from 0 to 52 MHz
- Optional 300 MHz 32-bit AHB bus
- Optional PCI specification 2.2 bus
- Optional APB bus
- Optional custom bus

## SD/SDIO Host IP Core

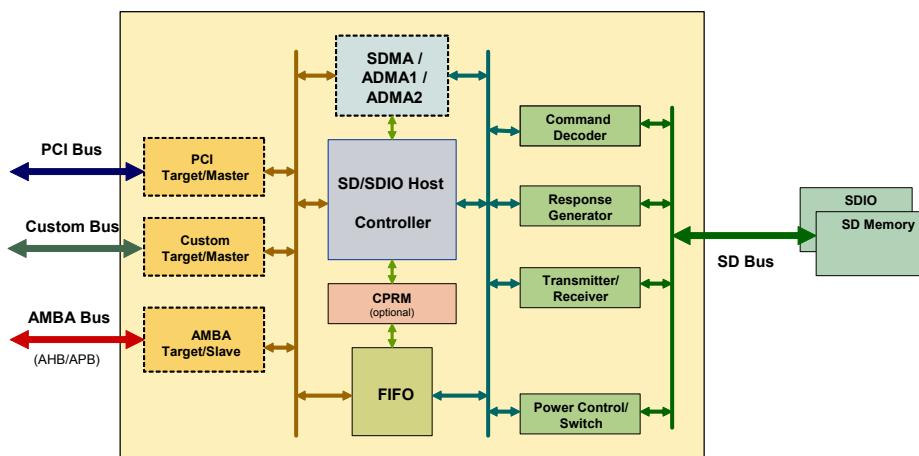
### Overview

The Arasan SD/SDIO Host IP Core controls communication between the SDIO Devices, SD Memory and MMC cards connected to the optional AHB, APB, PCI and custom buses. It is designed to support SD, SDIO and MMC applications in handheld and consumer electronic devices.

The Arasan SD/SDIO Host IP Core is fully compliant with the standard SD Host Controller Specification Version 2.0 Part A2 with SDMA (Single Operation DMA), ADMA1 (4-kbyte boundary limited DMA), and ADMA2 (scatter-gather DMA) support. ADMA2 allows data of any location and any size to be transferred in a 32-bit system memory. The Arasan IP core also supports multiple cards, SD1, SD4, SPI, high-speed, and full-speed transfer modes. In applications with an AHB interface, the Arasan SD/SDIO Host Version 2.0 IP Core communicates with the ARM processor at a clock speeds of 300 MHz. The SD/SDIO Host Controller provides a configurable FIFO to meet the requirements of customer applications. An optional CPRM functional block can be incorporated to perform a cipher algorithm for encryption and decryption.

The SD/SDIO Host IP Core is an RTL design in Verilog that implements an SD/SDIO Host Controller on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for verification. The Arasan SD/SDIO Host IP Core has been widely used in different SDIO applications by major chip vendors.

SD/SDIO Host IP Core Functional Block Diagram



# SD/SDIO Host IP Core

## SD Bus Interface Unit:

SD and SDIO devices communicate with the host controller through the SD Bus Interface Unit (BIU). The BIU consists of the Command Decoder, Response Generator, Transmitter/Receiver, and Power Control/Switch units. SD1, SD4, and SPI modes are supported. Other BIU functions includes the 16-bit CRC generator and checker for the data lines, 7-bit CRC generator and checker for the command and response lines, interrupt state machine, and BIU master state machine.

## AHB/APB Interface:

The Arasan SD/SDIO Host IP Core provides a Programmed IO method in which the ARM Host Driver transfers data using the Buffer Data Port Register. The AHB slave has direct access to the Host control registers and these registers can be programmed by the ARM processor through the AHB slave interface. Data transactions are performed through the AHB slave interface with Programmed IO method. The AHB Interface initiates a read or write transaction with the memory if the data transaction is an DMA data transfer.

## PCI Interface:

PCI Target/Master can be implemented that conforms to PCI specifications 2.2. The PCI Target/Master includes the DMA controller, configuration registers, PCI Power Management logic, and interrupt controller.

## DMA Controller:

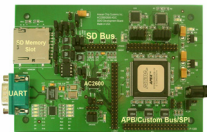
The SD host controller implements the scatter-gather DMA (ADMA2), 4 kbytes boundary limited DMA (ADMA1), and single operation DMA (SDMA) to provide flexible alternatives for different types of applications.

## Custom Interface:

General purpose buses such as 8-bit and 16-bit parallel buses are optional modules. Custom buses with special requirements can also be implemented.

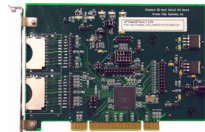
### Host Hardware Validation Platform (HVP):

The HVP is designed for validation and compliance testing of SD host devices .



### Host Hardware Development Kit (HDK):

The HDK is a PCI plug-in card for SD host prototyping and driver development.



## Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Optional Items:

- SD Host Hardware Validation Platform (HVP)
- SD Host Hardware Development Kit (HDK)
- SDIO Linux stack

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog



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## Data Sheet Links:

SD/SDIO Host IP Core:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)