

UniPro Controller IP Core

Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Unified Protocol (UniPro) is one in a family of standards addressing the mobile market.

The Arasan UniPro Controller IP core is fully compliant with the UniPro specification version 1.1 and supports the physical adapter layer of the D-PHY specification version 0.9. UniPro is a high-performance, chip-to-chip, serial interconnect bus for mobile applications. Designed to support up to 800 Mbps per data lane, it is scalable from one to four bidirectional lanes and a unidirectional clock lane, providing a maximum throughput of 3.2 Gbps. To achieve optimal performance the Arasan UniPro Controller implements the following layers in hardware: a) physical adapter layer, b) data link layer, c) network layer, and d) transport layer. TC0 and TC1 traffic classes are handled on a priority-based transmission, and additional features include support of multiple power modes, error detection and handling, and data transmission preemption. Unique to the Arasan controller is optional support that utilizes end-to-end flow control within UniPro to maximize transmission throughput and efficiency.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, UniPro provides the high-speed connectivity needed between the applications processor and application devices such as wireless modules, graphics processors, multimedia accelerators, and storage subsystems. Targeted specifically for mobile phones, UniPro will be the high-speed chip connection of choice moving forward.

The Arasan UniPro controller IP core utilizes an AHB system bus interface, but can be customized to support AXI, OCP, FIFO, or any variety of system interfaces needed for existing SoC developments. The IP core includes RTL code, test scripts, and a test environment for complete design verification.

Features

MIPI UniPro Compliant

- UniPro Version 1.1
- PPI for D-PHY
- MIPI D-PHY Version 0.9

Data Lanes

- Multi-lane: one to four data lanes
- Up to 800 Mbps per lane
- Maximum throughput: 3.2 Gbps

Transmission Support

- Packet-based protocol
- Device independent
- Handles all data types (control, isochronous, and bulk)
- Priority-based traffic classes (TC0 and TC1)
- Preemption support during data frame transmission
- Autonomous error detection and handling
- Multiple power modes

Layer Support

- PHY Adapter (L1.5)
- Data Link (L2)
- Network Layer (L3)
- Transport Layer (L4)

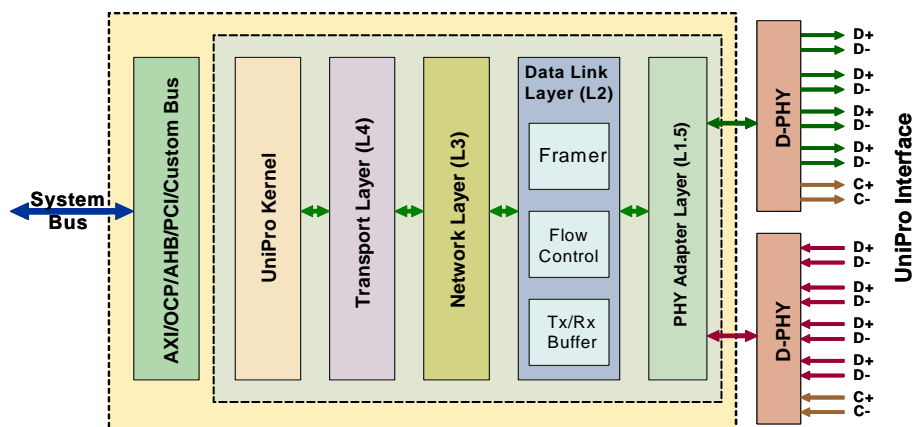
Interfaces

- AHB
- AXI
- OCP
- Custom

Options

- End-to-end flow control support
- Software stack

Arasan UniPro Controller IP Core - Functional Block Diagram



UniPro Controller IP Core

D-PHY:

The D-PHY operates in dual-simplex mode to support key UniPro features such as flow control and error recovery. The high-speed serial link employs a low-swing differential signaling technique for communication.

PHY Adapter Layer (L1.5):

The PHY Adapter Layer handles transmission and reception of DLL control symbols and data symbols via the D-PHY Lane Distributor and Merger in the multi-lane ports. The Adapter Layer supports MIPI UniPro power management operating modes, (re-)initialization of PHY Tx path, and transmission/reception of PHY symbols.

Data Link Layer (L2):

The Data Link Layer is responsible for frame composition and decomposition, frame pre-emption, flow control mechanism, 16-bit CRC generation and verification, detection of errors, autonomous error handling, and FC/NAC generation and reception. Two traffic classes are supported with priority-based arbitration. It also includes a Tx retry buffer and an Rx buffer.

Network Layer (L3):

The Network Layer supports addressing, packet composition and decomposition, and error handling. Two traffic classes (TC0 and TC1) are supported.

Transport Layer (L4):

The Transport Layer provides addressing, segment composition/decomposition, connection oriented data communication, end-to-end flow control, and error handling.

Application Interface (LA):

The Application Layer resides in the system that interfaces to the Arasan UniPro Controller IP. Logic or functionality of the Application Layer is unique to the particular application.

Device Management Entity (DME):

The DME interfaces to all protocol layers as well as the Application Layer. This layer handles the layer configuration parameters to and from the Management Information Base (MIB). It also gathers status from each layer and is responsible for the UniPro's reset behavior.

DMA:

The scatter-gather DMA supports linked-list or ring (chained) descriptors. The transmit and receive DMA operates independently. The skip length is programmable between descriptors for chained descriptors. Up to two buffers per descriptor are supported. A programmable interrupt structure is used for the DMA. Big or little endian operation is supported.

System Interface:

The Arasan UniPro Controller IP provides a variety of system interfaces to address the needs of different applications. The system interface controls the operation of the UniPro Controller IP. Interfaces such as AXI, OCP, AHB, PCI, or custom buses are available.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Tools:

- Software stack
- End-to-end flow control



Arasan Chip Systems, Inc.

1150 N. First St. Suite #201
San Jose CA 95112
Phone: 408-282-1600
Fax: 408-282-7800
E-mail: sales@arasan.com

Data Sheet Links:

UniPro Controller IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com