

SLIMbus™ Host Controller IP

Features

MIPI SLIMbus Compliant

- SLIMbus Version 1.0

Application Support

- Audio Systems
- Speakers
- Microphones
- Keypads
- GPS

Device Support:

- Generic devices: one or more
- Each generic device: 1 to 64 input/output ports
- Programmable ports

Transmission Support

- Maximum throughput: 28.8 Mbps
- Multiple concurrent sample rates on a single bus
- Reconfigurable data organization and data rates
- All data protocols supported
- Framer supports clock recovery mechanism
- Clock gearing – reduces bus power
- Dynamic clock frequency hopping
- Low clock rates and full clock pause
- All core messages
- Simple low-cost solution

I/O Modes

- DMA
- Programming
- FIFO

Host interfaces

- AXI
- AHB
- APB
- OCP
- Custom

Overview

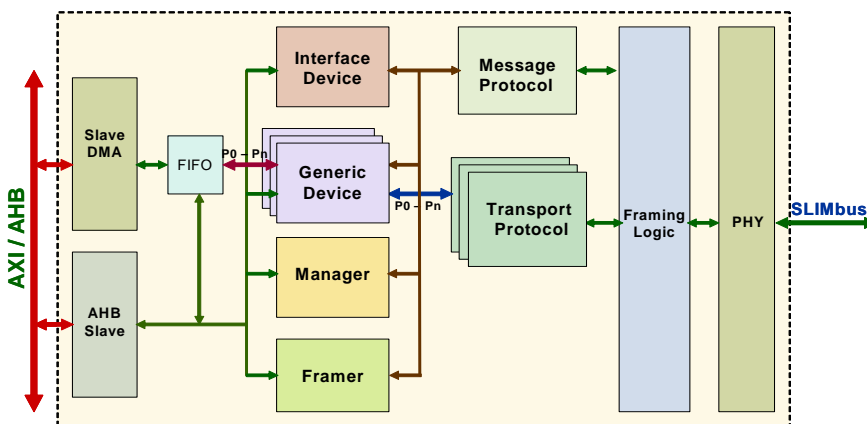
To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Serial Low-Power Inter-Chip Media Protocol (SLIMbus) is one in a family of standards addressing the mobile market.

The Arasan SLIMbus Host Controller IP core is fully compliant with the SLIMbus specification version 1.0. SLIMbus is a low-power, two-wire, multi-drop TDM bus that can support a wide variety of audio and digital devices to be connected simultaneously for mobile applications. Designed for a throughput of up to 28.8 Mbps, it is capable of supporting multiple devices on the system. Multiple generic devices can be supported, each having up to 64 I/O ports. The ports are programmable and support isochronous and extended asynchronous transport protocols. The manager performs configuration and controlling functions by sending control messages via the shared message channel. It is also responsible for assigning logical addresses to any device that is authorized to communicate on the bus. The framer is responsible for driving the clock signals and generating the SLIMbus frames. The SLIMbus Host also supports a special clock gear function to dynamically change clock frequencies to optimize bus power consumption.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, the SLIMbus Host provides universal connectivity needed between the applications processor and low-throughput devices in the system such as microphones, speakers, keypads, ringers, and Bluetooth devices.

The Arasan SLIMbus Host Controller IP core utilizes a master/slave AHB system bus interface, providing a high-performance host bus that addresses the needs of mobile and low-power applications. DMA and IO programming modes are supported. It can also be customized to support AXI, APB, OCP, or any variety of system interfaces needed for existing SoC development. The core includes RTL code, test scripts, and a test environment for complete design verification.

SLIMbus Host Controller IP Core - Functional Block Diagram



SLIMbus™ Host Controller IP

SLIMbus Manager:

SLIMbus manager is responsible for bus enumeration, bus configuration, dynamic channel allocation, assignment of logical addresses, bus initialization, controlling of devices, and other managing functions.

SLIMbus Framer:

The SLIMbus framer drives the clock line and places information on the data line required to establish the frame structure on the bus.

Generic Device:

The generic device provides single or multiple interfaces to external applications through the I2S, SPI, I2C, UART, parallel, or other custom buses. External input or output devices such as a MEMS microphone or cell phone can be connected to a selected I/O port. The generic device supports all transport protocols including isochronous and extended asynchronous transfers. The Arasan SLIMbus Host IP core supports multiple generic devices. Each generic device supports 1 to 64 I/O ports.

Framing Logic:

This block interleaves control channels and data channels into a single, serialized bit stream. It also splits the incoming bit stream into separate control and data streams.

Physical Layer Interface:

The physical layer interface is responsible for the transmission and reception of the SLIMbus bit stream between components. The physical layer drives the CLK and data lines using CMOS-like signals. The CLK line is unencoded, and the data line is encoded using Non-Return-to-Zero (NRZI) coding. The data line is driven on the positive edge and read on the negative edge of the CLK line. The CLK line has only two states.

System Interface:

The System Interface is a slave device that either transmits or receives data in response to commands from a master. It houses the operation registers. The interface can also have a slave DMA block to support DMA data transfers. The interface can be implemented with AHB, APB, AXI or OCP, adapting to the specific SoC and system requirement.

Custom Interface:

Other custom buses with special requirements can also be implemented.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Tools:

- Software Stack

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Data Sheet Links:

SLIMbus Host Controller IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com