

SLIMbus™ Device IP Core

Features

MIPI SLIMbus Compliant

- SLIMbus Version 1.0

Application Support

- Audio Systems
- Speakers
- Microphones
- Keypads
- GPS

Device Support

- Generic devices: one or more
- Each generic device: 1 to 64 input/output ports
- Programmable ports

Transmission Support

- Maximum throughput: 28.8 Mbps
- Multiple concurrent sample rates on a single bus
- Reconfigurable data organization and data rates
- All data transport protocols supported
- Framer supports clock recovery mechanism
- All core messages
- No external controller required
- Simple low-cost solution

Device Support

- I2S
- SPI
- I2C
- UART
- Parallel

Interfaces

- uC
- AHB
- Custom

Overview

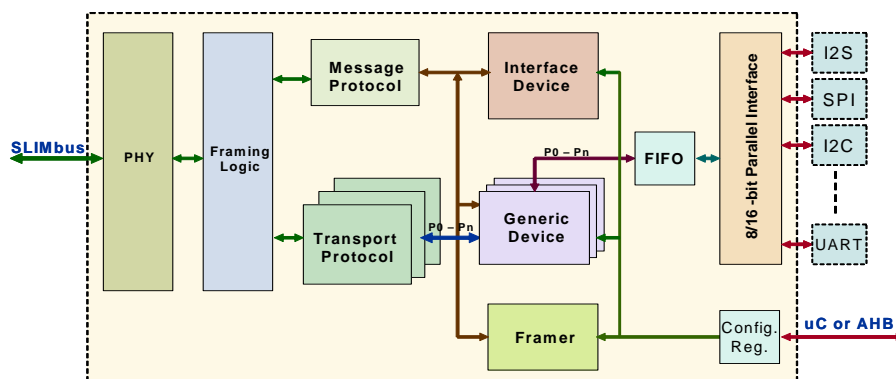
To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Serial Low-Power Inter-Chip Media Protocol (SLIMbus) is one in a family of standards addressing the mobile market.

The Arasan SLIMbus Device Controller IP core is fully compliant with the SLIMbus specification version 1.0. SLIMbus is a low-power, two-wire, multi-drop TDM bus that can support a wide variety of audio and digital devices to be connected simultaneously for mobile applications. Designed for a throughput of up to 28.8 Mbps, it is capable of supporting multiple devices on the system. The controller consists of a SLIMbus interface device and one or more SLIMbus generic devices. The interface device controls the frame layer and monitors message protocols implemented by the component. It also manages component reset so that a component can properly sequence its devices. The generic device provides bus management services for the component in which it resides. More than one generic device can be supported with each generic device supporting up to 64 I/O ports. The ports are programmable and support isochronous and extended asynchronous transport protocols. The SLIMbus generic device can provide multiple interfaces to external devices via the following bridge interfaces: a) I2S, b) SPI, c) I2C, d) UART, e) parallel, or f) custom interface. External devices such as a MEMS microphone or cell phone can be easily connected to any I/O port.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, SLIMbus provides universal connectivity needed between low-throughput devices in the system such as microphones, speakers, keypads, ringers, and Bluetooth devices. SLIMbus initialization and configuration are performed during system boot-up, eliminating the need for any external processor to manage the SLIMbus device.

The core includes RTL code, test scripts, and a test environment for complete design verification.

SLIMbus Device IP Core - Functional Block Diagram



SLIMbus™ Device IP Core

Interface Device:

The interface device provides bus management services for the component in which it resides. The interface device controls the frame layer and monitors message protocols implemented by the component. The interface device also manages component reset so that a component can properly sequence its devices. In addition, the interface device reports information about the status of the component.

Generic Device:

The generic device provides single or multiple interfaces to external applications through the I2S, SPI, I2C, UART, parallel, or other custom buses. External input or output devices such as a MEMS microphone or cell phone can be connected to a selected I/O port. The generic device supports all transport protocols including isochronous and extended asynchronous transfers. The Arasan SLIMbus Device IP Core supports multiple generic devices. Each generic device supports 1 to 64 I/O ports.

Framing Logic:

This block interleaves control channels and data channels into a single, serialized bit stream. It also splits the incoming bit stream into separate control and data streams.

Physical Layer Interface:

The physical layer interface is responsible for the transmission and reception of the SLIMbus bit stream between components. The physical layer drives the CLK and data lines using CMOS-like signals. The CLK line is unencoded, and the data line is encoded using Non-Return-to-Zero (NRZI) coding. The data is driven on the positive edge and read on the negative edge of the CLK line. The CLK line has only two states.

Parallel Interface:

The generic device provides an 8-bit or 16-bit parallel interface to applications connected to the SLIMbus device. Other interfaces such as I2S, SPI, I2C, UART, or custom interfaces can also be implemented.

Host Interface:

The Arasan SLIMbus Device IP provides a variety of system interfaces to address the needs of different applications. The system interface controls the operation of the SLIMbus Device IP. Interfaces such as a uC, AHB, or custom buses are available.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Tools:

- Software Stack

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Data Sheet Links:

SLIMbus Device IP Core:
www.arasan.com/datasheets/mipi.php

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www.arasan.com