Arasan
The Bus Stops Here

PRODUCT OVERVIEW

MIPI™ HSI Controller IP Core

Features

MIPI HSI Compliant

- HSI V1.0 Specification
- HSI Physical Layer Draft Version 1.1.00

Full-Duplex High Speed Serial Interface

- Up to Eight (8) logical transmit and receive channels

Configurable Channels

- Bandwidth – Throughput weighted per channel
- FIFO Size
- Transmission Bit Rate
- Transmission Modes
- Receiver Data Flow
- Slave DMA or PIO

Bit Transmission Modes (Tx and Rx)

- Stream Transmission Mode
- Frame Transmission Mode

Receiver Data Flow

- Synchronized Data Flow
- Pipelined Data Flow
- Receiver Real-time Data Flow

Maximum bandwidth:

- 200 Mbps in each direction (Full-duplex)

Transmit arbitration support

- Round-robin
- Priority-based

Mode support

- PIO mode
- SDMA mode

Data time out for receive operation

Clocking

- Clock Gearing – Mechanism to reduce power by clock control
- Dynamic clock frequency change - Optimizing bus power consumption
- Clock recovery mechanism – Receiver

Supports all HSI Commands

Interface Support

- AHB, APB, AXI, OCP & other custom buses

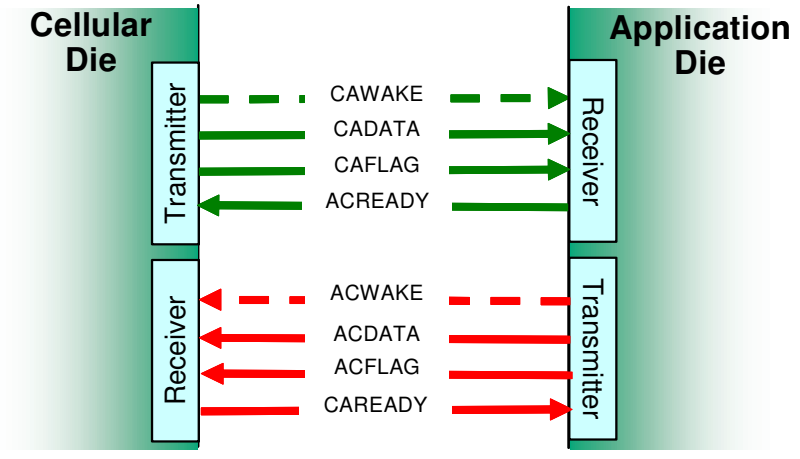
Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The High-speed Synchronous Serial Interface (HSI) is one in a family of standards addressing the mobile market.

HSI is a legacy MIPI specification widely used in a variety of products as a Baseband-application processor link. It is primarily intended to connect an application processor to a cellular modem controller in cellular handsets. The interface provides a low-latency communication channel over a chip-to-chip link by dividing the physical link to logical channels at the hardware level. Fundamentally, it is a point-to-point interface that can be considered to be two pairs of uni-directional transmitter-receiver pairs, where both pairs consist of two data signals and two control signals. HSI enables versatile, easy and simple serial link connections. It can reduce time to market and design cost of mobile handsets by simplifying serial chip-to-chip physical layer implementations.

The Arasan HSI controller IP core is compliant to the HSI 1.0 specification and 1.1 Physical layer draft. Supporting all HSI commands, it provides a host of configuration options to support easy integration into system requirements. It utilizes an OCP system bus interface, but can be customized to support AXI, AHB, FIFO, or any variety of system interfaces needed for existing SoC developments. The IP core includes RTL code, test scripts, and a test environment for complete design verification.

MIPI HSI IP Block Diagram



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Version 1.0a

HSI version 1.0 Compliant

HSI Controller IP Core

Tx Module

Tx modules consists of Tx frame creator and Tx frame driver blocks. The Tx frame creator generates a frame by appending the channel ID bits to the data from the Tx FIFO. The Tx frame driver block serializes the frame generated to the HSI IF.

Tx FIFO

The Tx FIFO provides data storage and can be configured and partitioned between 8 channels. A channel can be allotted anywhere from zero to the entire FIFO size. Each channel can be enabled or disabled via firmware.

Rx Module

The Rx module consists of a bit detector and analysis block. The detector de-serializes the data received. The analysis writes data into the buffer.

Rx buffer

The Rx buffer is configurable memory from the Rx block. This temporary buffer is used to avoid the head of line blocking during receive mode.

Rx FIFO

The Rx FIFO provides data storage and can be configured and partitioned between 8 channels. The controller interrupts the firmware when data is available to be read from the FIFO. The firmware can read the data by accessing Rx Data port registers of the Control registers block.

Control Registers

This block supports all the control registers of the HSI Controller.

Arbiter

The Arbiter manages the requests from all 8 channels. It can be programmed to a fixed or round robin priority. Based on priority, it manages the request from each channel.

Clock Generator

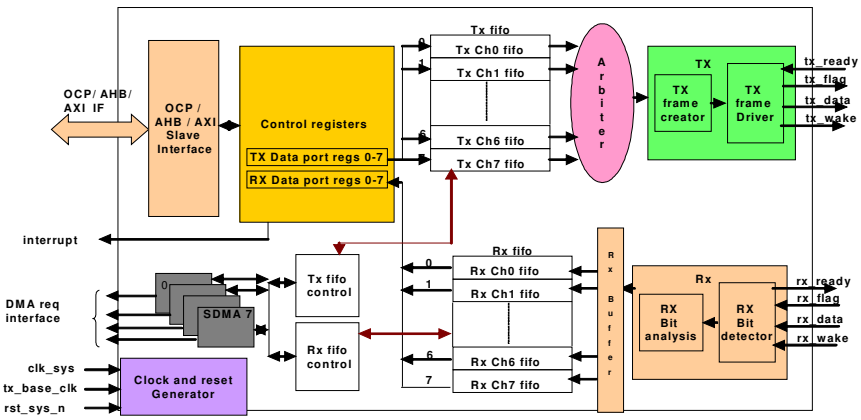
This generates clk_tx from clk_tx_base based on divisor value programmed in the Clock Control reg.

SDMA

The SDMA supports 8 channels. Transfer size, direction and the burst size are programmable.

System Interface

The Arasan HSI Controller IP provides a variety of system interfaces. The system interface controls the HSI operation and provides access to the FIFO. Interfaces such as OCP, AHB, AXI or a custom I/F can be easily implemented.



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Benefits:

- Fully compliant IP core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Tools:

- Simulation: ModelSim, VCS
- Synthesis: Synopsys Design Compiler

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Data Sheet Links:

MIPI IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com

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