Arasan
The Bus Stops Here

PRODUCT OVERVIEW

MIPI DSI Host IP Core™

Features

MIPI DSI Compliant

- DSI Version 1.01
- DPI Version 2.0
- DBI Version 2.0
- DSC Version 1.0a
- PPI for D-PHY
- MIPI D-PHY Version 0.9

Display, Resolution, Format Support:

- Multi-lane: one to four data lanes
- Virtual channels: one or two
- Resolution: QQVGA, QCIF, QVGA, CIF, VGA, and WVGA
- Pixel format: RGB565, LRGB565, RGB666, and RGB888

Mode and Packet Support

- Command and video mode support (type 1, 2, 3, and 4 display architecture)
- Mode switching: low power and ultra low power
- Burst mode: dual video channel
- Non-burst mode: single video channel
- Bus turnaround
- 80 Mbps to 1 Gbps per lane
- Fault error recovery scheme

IP Options

- DPI: pixel stream transfers
- DBI: pixel stream and command transfers
- AHB: processor bus interface
- Enhanced Resolution: XGA

Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Display Serial Interface (DSI) is one in a family of standards addressing the mobile market.

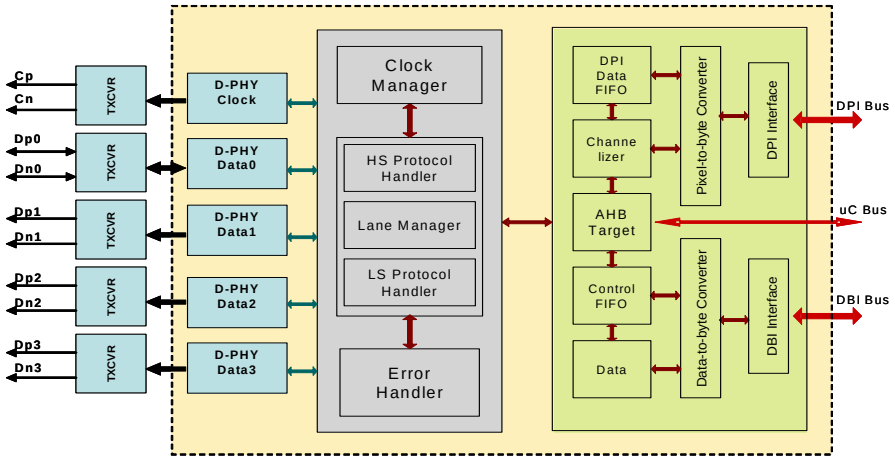
The Arasan DSI Host IP core is fully compliant with the DSI specification version 1.01 and supports the physical adapter layer of the D-PHY specification version 0.9. DSI is a high-speed, high-resolution, serial interconnect bus offering connectivity to video display devices such as monitors, media players, and cell phone displays. Adopting existing industry pixel and display formats, the DSI Host IP core complies with the MIPI DPI version 2.0, DBI version 2.0, and DCS version 1.0a specifications, making DSI or DPI transactions over DSI transparent to the system. The DSI core is designed such that it can be customized to support DSI, DPI, or both if desired.

Designed to support from 80 Mbps up to 1 Gbps per data lane, it is scalable from one to four data lanes and a clock lane, providing a maximum throughput of 4 Gbps. The DSI host core is capable of supporting a variety of resolutions and formats from QQVGA to WVGA and RGB565 to RGB888. More importantly, Arasan has provided enhanced capability to support resolutions beyond the DSI specification of WVGA, to XGA. The DSI can support both command and video modes providing the greatest range of flexibility. It is also designed for up to two virtual channels to accommodate multiple displays.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, the DSI Host IP core provides a complete solution for mobile digital display applications in mobile phones and portable PCs.

The Arasan DSI Host IP core utilizes an AHB system bus interface, but can be customized to support AXI, PCI, or any variety of system interfaces needed for existing SoC developments. The core includes RTL code, test scripts and a test environment for complete design verification.

DSI Host IP Core - Functional Block Diagram



Version 1.2a

mipi alliance member

MIPI DSI Host IP Core™

Protocol Layer:

Protocol layer bytes are organized into defined groups called packets. The protocol defines required headers for each packet and how header information is generated and interpreted. The transmitting side of the interface appends header and error-checking information to data being transmitted. On the receiving side, the header is stripped off and interpreted by corresponding logic in the receiver. Error checking information is used to test the integrity of incoming data.

Lane Management Layer:

DSI is a lane scalable interface. Applications running more bandwidth than that provided by one data lane may expand the data path to two, three, or four lanes and obtain approximately linear increases in peak bus bandwidth. The transmitting side of the interface distributes a sequence of packet bytes across enabled lanes. On the receiver side, the layer collects incoming bytes and consolidates the bytes into complete packets to pass into the following packet decomposer. The number of data lanes can be programmed via the AHB register. It also provides logic to drive the clock and data lanes of the D-PHY.

ECC:

ECC is always generated and appended in the packet header from the transmitter logic of the DSI host. Generating and sending ECC from DSI peripherals to the host is optional. The error correcting code used by DSI is a 7+1 bit Hamming-modified code (72,64), allowing for protection of up to sixty-four data bits. A seven-bit Hamming code can correct a single-bit error or detect a two-bit error, but is not capable of doing both simultaneously, so one extra parity bit is added.

Error Handler:

The error handler deals with errors in low-power mode due to contention. It also includes timers to manage high-speed transmit timeout and timers for contention recovery during low-speed reception.

Display Pixel Interface (DPI):

An external display device links to the display host processor via the Display Pixel Interface. Controls are derived from short packets, and pixel data is fed from long data packets. The DPI interface has FIFO controller logic to derive video patterns for corresponding signal assertions for every pixel clock at the DPI interface. Control data and payload data are stored in the control FIFO and DPI Data FIFO respectively.

DPI Data FIFO:

The DPI interface uses a 4 Kbyte FIFO to support the streaming of 1024 x 768 video. The 4 Kbyte FIFO is big enough to store a 24-bit 1024-pixel scan line. The size of the DPI FIFO can be customized.

Display Bus Interface (DBI):

DBI supports display modules having display controllers and frame buffers. Outgoing images and commands are loaded into the DBI FIFO and Control FIFO respectively by the display host processor. Video, command, and timing data is sent through the DSI link to one to four DSI devices using either burst mode or non-burst mode.

DBI Data FIFO and Control FIFO:

The DBI interface uses a 4 Kbyte FIFO to support the streaming of 1024 x 768 video. The 4 Kbyte FIFO is big enough to store a 24-bit 1024 pixel scan line. The size of the DBI FIFO can be customized. The Control FIFO holds commands and video timing information.

AHB Interface:

The AHB interface connects the Arasan DSI Host IP Core to an external AHB processor. It also drives the 32-bit data and 32-bit address buses. This interface mainly handles programming the core for initial operations and also for monitoring errors that occur on the PHY lanes. Other custom bus interfaces are also available.

Benefits:

- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

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Data Sheet Links:

MIPI DSI Host IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com