

Features

MIPI DSI Compliant

- DSI Version 1.01
- DPI Version 2.0
- DBI Version 2.0
- DCS Version 1.0a
- PPI for D-PHY
- MIPI D-PHY Version 0.9

Display, Resolution, Format Support:

- Primary and secondary displays
- Multi-lane: one to four data lanes
- Virtual channels: one to four
- Resolution: QQVGA, QCIF, QVGA, CIF, VGA, and WVGA
- Pixel format: RGB565, LRGB565, RGB666, and RGB888

Mode and Packet Support

- Command and video mode support (Type 1, 2, 3, and 4 display architecture)
- Mode switching: Low power and ultra low power
- Burst mode: single video channel
- Non-burst mode: dual video channel
- Multiple packets per transmission
- Acknowledge packets and trigger messages
- All generic read/write, short and long packets
- Bus turnaround
- Programmable error injection and detection
- EOT, ECC, and CRC enable/disable mechanisms
- Generic parallel interface for sending and receiving vendor-specific information to display unit
- Fault error recovery scheme
- High Speed (HS): 800 Mbps
- Low Power (LP): 10 Mbps
- Reverse LP transmission
- Contention recovery
- Interleaved Data Stream

IP Options

- DPI: pixel stream transfers
- DBI: pixel stream and command transfers
- AHB: processor bus interface
- Enhanced Resolution: XGA

MIPI DSI Device IP Core

Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Display Serial Interface (DSI) is one in a family of standards addressing the mobile market.

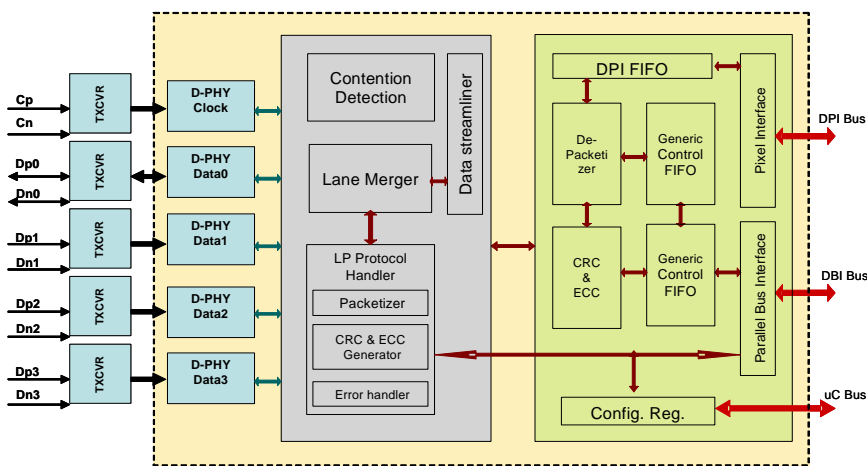
The Arasan DSI Device IP core is fully compliant with the DSI specification version 1.01 and supports the physical adapter layer of the D-PHY specification version 0.9. The DSI Device IP core is a high-speed, high-resolution, serial interconnect bus designed for display peripheral devices in mobile phones, media players and portable display units. Adopting existing industry pixel and display formats, the DSI Device IP core complies with the MIPI DPI version 2.0, DBI version 2.0, and DCS version 1.0a specifications, making DSI or DPI transactions over DSI transparent to the system. This makes supporting traditional or legacy systems an easy feat. The DSI core is designed to be customized to support DSI, DPI, or both to interface with various display devices.

Designed to support from 80 Mbps up to 1 Gbps per data lane, it is scalable from one to four data lanes and a clock lane, providing a maximum throughput of 4 Gbps. The DSI Device core is capable of supporting a variety of resolutions and formats from QQVGA to WVGA and RGB565 to RGB888. More importantly, Arasan has provided enhanced capability to support resolutions beyond the DSI specification of WVGA, to XGA. The DSI can also support both command and video modes providing the greatest range of flexibility. Up to four DSI Device IPs (virtual channels) can be connected to an Arasan DSI Host.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, the DSI Device IP core provides a complete solution for mobile digital display applications in mobile phones and portable PCs.

The Arasan DSI Device IP core utilizes an AHB system bus interface, but can be customized to support AXI, PCI, or any variety of system interfaces needed for existing SoC developments. The core includes RTL code, test scripts, and a test environment for complete design verification.

DSI Device IP Core - Functional Block Diagram



MIPI DSI Device IP

Protocol Layer:

The Protocol Layer defines the packet headers and how header information is generated and interpreted. The Protocol Layer depacketizes data bytes in the transmitting and receiving directions. This layer maintains the data integrity by using an error checking mechanism. The ECC unit performs checking and correction of the incoming packets to ensure that the data is free from errors. The CRC checker unit detects checksum errors to provide additional data protection.

Lane Management Layer:

DSI is a scalable lane interface. Applications running more bandwidth than that provided by one data lane may expand the data path to support two, three, or four lanes. In doing so, approximately a linear increase in peak bus bandwidth can be obtained. The transmitting side of the interface distributes a sequence of packet bytes across the enabled lanes, where each lane is an independent block of logic and interface circuitry. On the receiving side, the layer collects incoming bytes from the enabled lanes and consolidates the bytes into complete packets before passing the data to the following packet decomposer.

DBI Interface:

The DBI interface links the IP core to external display devices. Controlling functions are generated by the DCS or by generic commands read from the control FIFO. For a DCS long write command, the command stored at the first location of the data FIFO is sent to the DBI interface, and the associated data listed in the word count field of the control FIFO is passed to the DBI interface for the data phase. For a DCS read command, the number of data bytes collected for the DBI read operation

depends on the maximum return packet size defined in the register settings. The maximum data transfer size of a generic command is one Kbyte. The DSI core uses two dual-port FIFOs for performing read and write transactions for payload and control data. Both FIFOs are used at the same time to achieve maximum throughput.

DPI Interface:

The DPI interface links the IP core to external display devices. Controlling functions are generated once the short packets that carry the DPI events are decoded to signal to the pixel interface as frame, blanking, or line timing information. Data bytes that are sent via long data packets are directed to the data FIFO and streamlined for processing. Based on the header information that accompanies each long packet, the data is converted to pixels and sent to the active matrix display. Pixel data is stored in a dual-port FIFO along with its data type information, and the associated pixel data is set in the word count field.

Micro Controller Interface:

The micro controller bus allows the host processor to control the configuration and functionality of the DSI Device IP. Optional microprocessor interfaces include AHB, AXI, PCI, and custom buses.

Benefits:

- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

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Data Sheet Links:

MIPI DSI IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com