

MIPI CSI-2 Transmitter IP Core

Features

MIPI CSI-2 Compliant

- CSI Version 1.0
- PPI for D-PHY
- MIPI D-PHY Version 0.9

Transmission Support

- Multi-lane: one to four data lanes
- Modes (high speed (HS), low power (LP), ultra low power, escape, and control)
- HS mode: 80 Mbps to 1 Gbps synchronous
- LP mode: 10 Mbps asynchronous
- LP mode: spaced one-hot encoding for data
- Controls to start and re-start data transmissions
- 4 Kbyte cut-through FIFO: transfer of 64 Kbyte payload
- DMA with per-packet interrupt
- Sequential or random read/write access of registers
- I2C interface to control camera functions
- Sensor camera interface for image byte-to-pixel conversion

System Interface

- uC
- AHB
- AXI
- PCI
- Custom

Overview

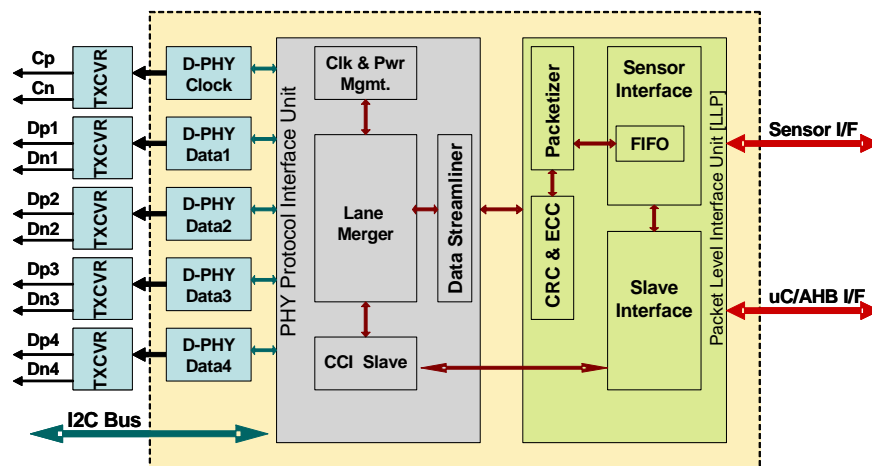
To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Camera Serial Interface (CSI) is one in a family of standards addressing the mobile market.

The Arasan CSI-2 Transmitter IP core is fully compliant with the CSI-2 specification version 1.0 and supports the physical adapter layer of the D-PHY specification version 0.9. CSI-2 is a high-performance serial interconnect bus for mobile applications connecting digital imaging modules like a host processor or image processor to camera sensors. Designed to support from 80 Mbps up to 1 Gbps per data lane, it is scalable from one to four data lanes and a clock lane, providing a maximum throughput of 4 Gbps. The CSI-2 Transmitter core can manage up to four data lanes through the lane management and packetizer units. The transmitter allows captured data from the camera sensor in JPEG, MPEG, RAW, YUV, and RGB formats to be transferred to the receiver unit where the processor can manage and manipulate the data; for example, image format conversion. The camera control interface (CCI) bus slave allows control communications via the I2C control bus. All CCI registers are memory mapped to the host processor bus to support different CSI-2 receiver devices.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, the CSI-2 Transmitter IP core provides a complete solution for mobile digital camera applications in mobile phones and portable PCs.

The Arasan CSI-2 Transmitter IP core utilizes an AHB system bus interface, but can be customized to support a uC, AXI, or any variety of system interfaces needed for existing SoC development. The IP core includes RTL code, test scripts, and a test environment for complete design verification.

CSI-2 Transmitter IP Core - Functional Block Diagram



MIPI CSI-2 Transmitter IP Core

PPI/Lane Management Unit:

This layer acts as the lane buffer and distributes the data across different lanes and manages the data and error controls for each lane.

PLI/Low Level Protocol Unit:

This layer packetizes the data stream with respect to channels, frames, colors, and line formats. An ECC generation unit adds error correction code in the packetized data. A CRC generator unit introduces CRC checksum bits for additional payload data protection.

Pixel/Byte Packing formats:

Porting of pixel formats to data bytes in the payload data is done depending on the type of image data supported by the application. This layer packs data format to bytes for the low-level protocol layer.

Sensor Interface:

The sensor interface transfers data between the CSI device and the camera sensor.

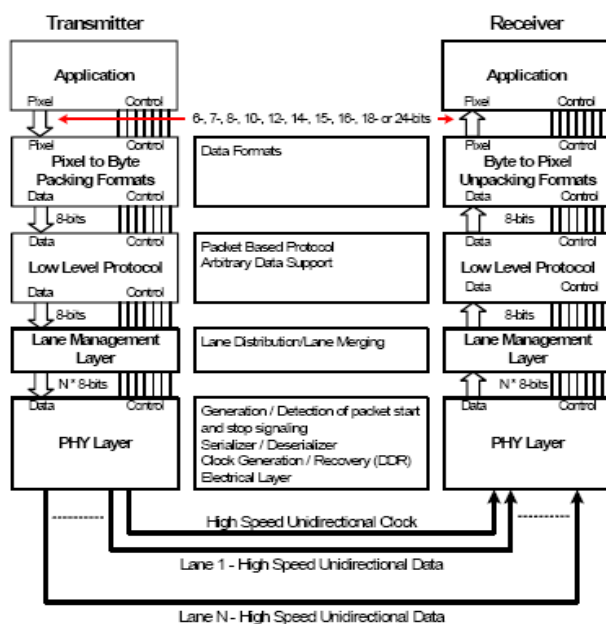
System Interface:

A variety of system interfaces such as a uC, AHB or custom interface can be provided to control operation of the CSI device.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant Verilog code ensured using Spyglass

The MIPI CSI protocol layers



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Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents



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Data Sheet Links:

CSI-2 Transmitter IP core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com