

MIPI CSI-2 Receiver IP Core

Features

MIPI CSI-2 Compliant

- CSI-2 Version 1.0
- PPI for D-PHY
- MIPI D-PHY Version 0.9

Transmission Support

- Multi-lane: one to four data lanes
- Modes (high speed (HS), low power (LP), ultra low power, escape, and control)
- HS mode: 80 Mbps to 1 Gbps synchronous
- LP mode: 10 Mbps asynchronous
- LP mode: spaced one-hot encoding for data
- 4 Kbyte cut-through FIFO: transfer of 64 Kbyte payload
- I2C controlled through AHB/AXI interface
- Image signal processor interface for image format conversion and pixel-to-byte conversion

System Interface

- uC
- AHB
- AXI
- PCI
- Custom

Overview

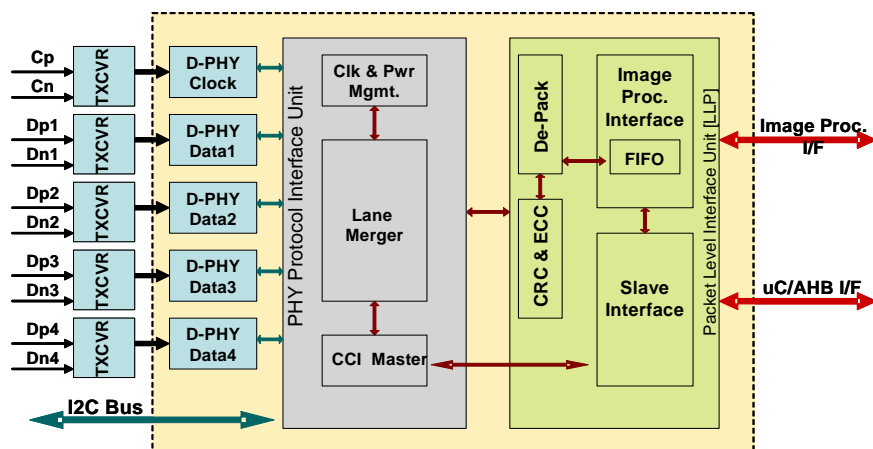
To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Camera Serial Interface (CSI) is one in a family of standards addressing the mobile market.

The Arasan CSI-2 Receiver IP core is fully compliant with the CSI-2 specification version 1.0 and supports the physical adapter layer of the D-PHY specification version 0.9. CSI-2 is a high-performance serial interconnect bus for mobile applications connecting camera sensors to digital imaging modules like a host processor or image processor. Designed to support from 80 Mbps up to 1 Gbps per data lane, it is scalable from one to four data lanes and a clock lane, providing a maximum throughput of 4 Gbps. The CSI-2 Receiver core can manage up to four data lanes through the lane management and de-packetization units. It accepts transmitted data from the camera sensor and sends it to the image processor for conversion and processing to pixel format, JPEG, or MPEG. For example, byte to pixel conversion or picture viewing applications or image format conversions can be transferred to the host processor via the AHB or AXI bus or directly to an image processor. The camera control interface (CCI) bus master handles the image transmission via an I2C control bus. The I2C register values and functions can be programmed via the AHB or AXI interface.

Designed specifically for applications such as mobile phones, portable handheld media players, and mobile terminals, the CSI-2 Receiver IP core provides a complete solution for mobile digital camera applications in mobile phones and portable PCs.

The Arasan CSI-2 Receiver IP core utilizes an AHB system bus interface, but can be customized to support a uC, AXI, or any variety of system interfaces needed for existing SoC development. The IP core includes RTL code, test scripts, and a test environment for complete design verification.

MIPI CSI-2 Receiver IP Core - Functional Block Diagram



MIPI CSI-2 Receiver IP Core

PPI/Lane Management Unit:

This layer is capable of managing one to four lanes according to the programmability criteria. This unit merges data gathered from different lanes, combines them into a single data stream, and forwards them to the LLP/ PLI unit.

PLI/Low Level Protocol Unit:

This layer de-packetizes the data stream with respect to channels, frames, colors, and line formats. An ECC correction unit recovers data in the packet headers to ensure that the data is free from errors. An included CRC checker detects CRC checksum errors for additional data protection.

Byte/Pixel Packing Formats:

The byte/pixel packing unit converts data bytes from the low-level protocol unit to a pixel format used by the application layer.

Image Processor Interface:

The image processor interface transfers data between the CSI device and the image processor. Data can be easily transferred for image processing.

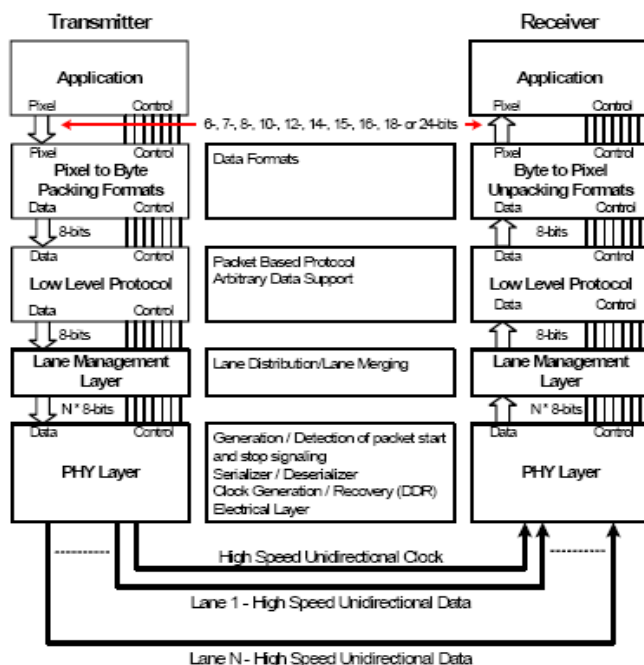
System Interface:

The Arasan CSI-2 IP provides a variety of system interfaces to address the needs of different applications. Interfaces such as a uC, AHB, or custom buses are available.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant Verilog code ensured using Spyglass

The MIPI CSI protocol layers



Deliverables:

- RMM-compliant synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

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Data Sheet Links:

MIPI CSI-2 Receiver IP Core:
www.arasan.com/datasheets/mipi.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com