Arasan
The Bus Stops Here

PRODUCT OVERVIEW

MIPI CSI-2 Receiver IP Core

Features

MIPI CSI-2 Compliant
- CSI-2 Version 1.0
- PPI for D-PHY
- MIPI D-PHY Version 0.93

Transmission Support
- Multi-lane: 1 to 4 lanes
- Mode Support
- High speed (HS)
- Low power (LP)
- Ultra low power
- Escape
- Control
- HS mode: 80 Mbps to 1 Gbps synchronous
- LP mode: spaced one-hot encoding for data
- Once byte buffer for both data-in path
- 4K byte cut-through FIFO: transfer of 64K byte payload
- Automated DMA with per packer interrupt
- I2C controlled through AHB/AXI interface
- Image signal processor interface for image format conversion and pixel to byte conversion
- AHD/AXI master interface for high speed payload data transfers

Optional Interface
- AHB
- AXI
- PCI
- Custom

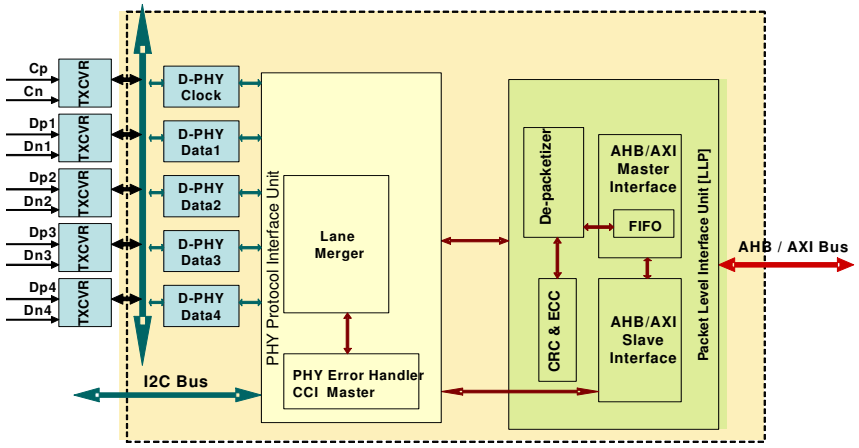
Overview

To address the explosive growth in the mobile industry, the Mobile Industry Processor Interface (MIPI) Alliance was created to define and promote open standards for interfaces to mobile application processors. The Camera Serial Interface (CSI) in one in a family of standards addressing the mobile market.

The Arasan CSI-2 Receiver IP core is fully compliant to the CSI-2 specification version 1.0 and supports the physical adapter layer of the D-PHY specification version 0.93. CSI-2 is a high performance serial interconnect bus for mobile applications connecting camera sensors to digital imaging modules like a host processor or image processor. Designed to support from 80 Mbps up to 1 Gbps per data lane, it is scalable from 1 to 4 data lanes and a clock lane, providing a maximum throughput of 4 Gbps transfer rate. The CSI-2 Receiver core can mange up to 4 data lanes through the lane management and de-packetization units. It accepts transmitted data from the camera sensor and sends it to the image processor for conversion and processing to pixel format, JPEG, or MPEG. For example, byte to pixel conversion or picture viewing applications or image format conversations can be transferred to the host processor via the AHB or AXI bus. The camera control interface (CCI) bus master handles the controls image transmission via an I2C control bus.

Designed specifically for applications such as the mobile phone, portable handheld media players or mobile terminals, the CSI-2 Receiver IP core provides a complete solution for mobile digital camera applications in mobile phones, portable PC's and such products.

MIPI CSI-2 Receiver IP Core Functional Block Diagram



Version 1.2

mipi alliance member

MIPI CSI-2 Receiver IP Core

PPI/Lane Management Unit:

This layer is capable of managing 1 to 4 four lanes according to the programmability criteria. This unit merges data gathered from different lanes, combines them to a single data stream, and forwards them to the LLP/ PLI unit.

PLI/Low Level Protocol Unit:

This layer de-packetizes the data stream with respect to channels, frames, colors and line formats. An ECC correction unit recovers data in the packet headers to ensure that the data is free from errors. An included CRC checker detects CRC checksum errors for additional data protection.

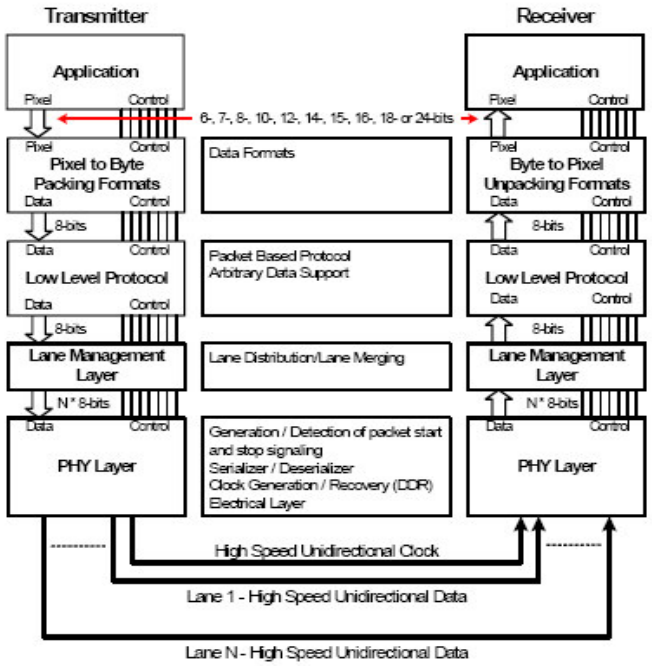
Byte/Pixel packing formats:

The Byte/Pixel packing unit converts data bytes from the low level protocol unit to a pixel format used by the application layer.

AHB / AXI Interface:

The AHB / AXI master transfers data between the host processor and MIPI CSI-2 Receiver. Data received by the CSI-2 Receiver can be sent to the host processor for image format conversion. The AHB / AXI master includes a FIFO for high-speed DMA transfer. Automated DMA is supported.

The MIPI CSI protocol layers.



Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant Verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Arasan
The Bus Stops Here

Arasan Chip Systems, Inc.

2010 N. First St. Suite #510
San Jose CA 95131
Phone: 408-282-1600
Fax: 408-282-7800

Data Sheet Links:

MIPI CSI-2 Receiver IP Core:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com