

Features

Compliance

- USB specification revision 2.0
- EHCI specification revision 1.0

USB 2.0 Host

- Supports up to 127 devices and 8 downstream ports
- OHCI companion processor for USB 1.1 transfers
- 16-bit UTMI and 8-bit ULPI interfaces
- Direct addressing all IP core registers from AHB, PCI, or custom bus
- DMA controller supports high-speed data transfers between USB Host IP and host bus

Host Interface

- 8, 16, or 32-bit host bus
- Optional 133 MHz AHB Rev. 2.0 master/slave interface
- Optional 33 MHz PCI Rev. 2.2 master/target interface
- Optional custom bus interface

USB 2.0 Host IP

Overview

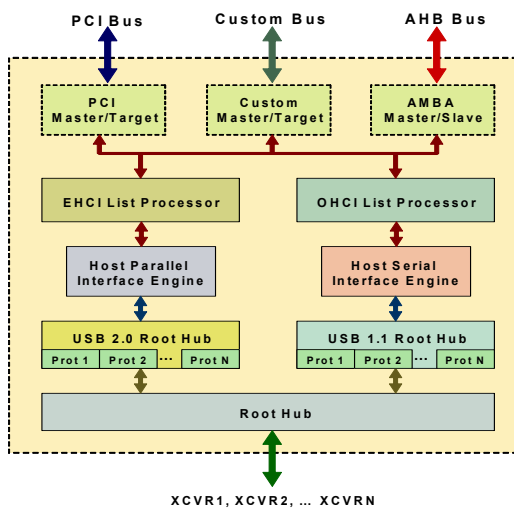
The Arasan USB 2.0 Host IP is an USB 2.0 specification compliant host IP core with an optional AHB, PCI, or custom host interface. The USB 2.0 Host IP supports 480 Mbit/s in High Speed (HS) mode, 12 Mbit/s in Full Speed (FS) mode, and 1.5 Mbit/s in Low Speed (LS) mode.

The IP consists of an Enhanced Host Controller Interface (EHCI) and a companion Open Host Controller Interface (OHCI). The EHCI processor handles HS transactions and is the default owner of the root hub that connects to the downstream ports. In a downstream data transfer, the EHCI sends data to the Host Parallel Interface Engine (HPIE) for encoding and CRC appending. Data received by the USB 2.0 Root Hub is forwarded to the downstream ports. Similarly, FS and LS transactions are handled by the OHCI, Host Serial Interface Engine (HSIE), and USB 1.1 Root Hub. The Root Hub performs multiplexing and forwarding of packets between the downstream ports and USB 2.0/1.1 Root Hubs. Up to 8 downstream ports can be connected to the USB 2.0 Host IP core.

With the addition of an optional ULPI Wrappers, the Arasan USB 2.0 Host IP core can be connected directly to a 16-bit standard UTMI or 8-bit ULPI transceiver.

The Arasan USB 2.0 Host IP core is an RTL design in Verilog that implements an USB host controller on an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verification.

USB 2.0 Host IP Core Functional Block Diagram



USB 2.0 Host IP

Optional AHB Interface:

The AHB master/slave interface provides a high-speed connection between the AHB host and USB 2.0 host controller. When operating as an AHB slave, the DMA controller can be used to manage the high-speed data transfers.

The AHB host has direct access to all registers in the USB 2.0 Host IP. Configuration and operations of the USB host can be controlled by an AHB host through the AHB interface.

Optional PCI Interface:

An optional PCI version 2.2 master/target interface allows a PCI host to access all registers in the USB 2.0 Host IP. The PCI interface supports programmable I/O and DMA data transfer methods. In programmable I/O method, the PCI host driver transfers data using the Buffer Data Port register. In DMA method, the DMA controller is the bus master during the data transfer. The PCI master/target interface also supports Power Management conforming to the PCI power management interface specification.

Optional Custom Interface:

Custom bus with special requirements such as a bus width from 4-bit to 64-bit can be provided by Arasan Chip Systems. The custom bus can be used to support processors such as 8051. A DMA controller can also be included as an optional module. Host processor connected to the custom bus has direct access to

all registers in the USB 2.0 Host IP. Configuration and operation of the USB host core can be controlled by the host processor.

UTMI Interface:

The Arasan USB 2.0 Host IP core implements a 16-bit UTMI compliant module that provides a seamless interface to standard interface components such as the Philips USB 2.0 UTMI transceiver.

ULPI Interface:

The Arasan USB 2.0 Host IP core provides an optional UTMI to ULPI wrapper. Instead of using a high pin count UTMI interface, user may choose to use an ULPI interface to reduce the pin count to 12.

Supported OS for Device Drivers:

WinXP, and, Linux.

Custom Design Services:

Arasan Chip Systems is experienced in providing custom design services including logic, SoC, system and software designs.

Benefits

- Fully compliant USB 2.0 core
- Premier direct support from Arasan IP core designers
- Hardware Evaluation Kit available

Deliverables

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Item:

- Evaluation board available



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Data Sheet Links:

USB 2.0 Host IP:
http://www.arasan.com/usb2_host.pdf

For a complete directory of Arasan IPs, please visit:
www.arasan.com