

SLIMbus™ Host/Device Verification IP

Features

- Functional verification, validation, and compliance testing of SoC or ASIC designs
- Easy-to-use test environment
- Meets SLIMbus standard specification version 1.0
- Two-wire interface supporting audio, data, and bus / device control
- Single bus supports multiple audio and low / mid - speed data devices
- Embedded manager for SLIMbus control
- Embedded framer allows clock source operation using 24 MHz and 25 MHz root frequencies
- Embedded interface for component-wide error reporting
- Supports two Generic Devices for supporting audio and voice data flows
- Each Generic Device has two ports (one input and one output)
- Each port supports Isochronous, Pushed, Pulled, and Locked transport protocols
- Data sample sizes of 8, 16, 24, or 32 bits
- Dynamic SLIMbus clock frequency scaling and clock pausing minimizes power consumption
- Configurable data rates and organizations on the fly
- Very low clock rates and full clock pause are supported
- Multiple concurrent sample rates on a single bus
- Programmable ports
- Framer supports clock recovery mechanism
- Supports all core messages
- User-friendly monitor

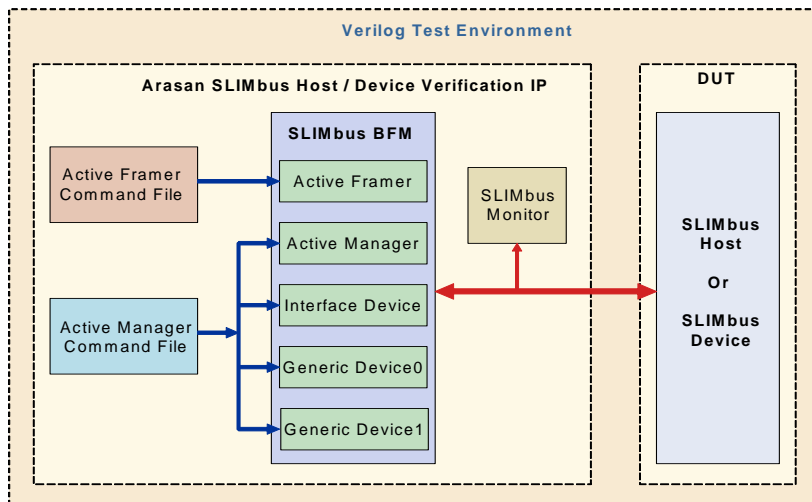
Overview

The Arasan SLIMbus Verification IP is a comprehensive test environment for verification, validation, debugging, and testing of SLIMbus host or SLIMbus device applications for functionality, compliance, or interoperability. The SLIMbus Verification IP allows the complete and extensive testing of a SLIMbus host or SLIMbus device application, it also ensures full functionality of the SoC or ASIC before the design is finalized.

The Arasan SLIMbus Host / Device Verification IP consists of the SLIMbus 1.0 behavior functional model (BFM), Command Files, Input Data Files, Output Data Files, and SLIMbus monitor. The Command File provides a comprehensive set of test vectors as well as a complete set of SLIMbus 1.0 compliant commands for extensive testing, validation, or debugging. The test environment also supports users defined data / command generation as well as error injection.

The SLIMbus Verification IP is delivered with an interconnected host and device test environment, the same setup supports the verification and testing of SLIMbus device IPs as well as SLIMbus host IPs. The verification IP is an RTL design in Verilog.

SLIMbus Device IP Core Functional Block Diagram



SLIMbus™ Host/Device Verification IP

SLIMbus Functional model:

The SLIMbus functional model (BFM) consists of the Active Framer, Active Manager, Interface device, Generic Device0, and Generic Device1.

Active Manager:

The Active Manager Command File emulates the function of an Active Manager when Active Manager model in SLIM BFM is enabled. It also initiates the transmission of messages and transactions by performing tasks in active_manager_cmd.v. The Active Manager emulates the function of a Slim -Device when Active Manager Model in SLIM BFM is disabled.

Active Framer:

Active Framer Command File emulates the function of an Active Framer when the Active Framer model in SLIM BFM is enabled. It also initiates the transmission of messages by performing tasks in active_framer_cmd.v

Generic Devices:

The Generic Devices emulates the func-

tion of the Generic Devices in SLIM BFM by performing tasks in active_manager_cmd.v

Interface Device:

The Interface Device emulates the function of an Interface Device in SLIM BFM by performing tasks in active_manager_cmd.v

SLIMbus Monitor:

The SLIMbus Monitor records the activities of the bus that connects the Arasan Host/Device Verification IP and the DUT. The SLIMbus monitor is a passive device that does not affect the operation of the DUT in any way.

Command, Input and Output Files:

The Command File consists of a list of SLIMbus messages and test cases. The Command File provides inputs to the SLIMbus BFM for configuration, functions initiation, testing, and debugging. The test environment also supports users defined data / command generation as well as error injection.

Benefits:

- Fully compliant test environment
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- Verilog RTL source test bench
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

SLIMbus Device IP Core:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit: www.arasan.com