Arasan
The Bus Stops Here

PRODUCT OVERVIEW

SD/SDIO Host/Device Verification IP

Features

- Functional verification, validation, and compliance testing of SoC or ASIC designs
- Easy-to-use test environment
- Meets standard SD Host Controller Specification Version 2.0 Part A2
- Meets SDIO Device v2.0 Specification Part E1
- Supports SD High Capacity (SDHC) and SD High Speed (SDHS) cards standards
- Supports force event testing with Test Registers
- Up to 7 functions in SPI, SD1, or SD4 mode
- Host clock rate from 0 to 50 MHz
- Hardware interrupt to host
- Maximum 200 Mbit/s read/write with 4-bit data lines in SD4 mode
- CRC7 and CRC16 modules
- Supports direct R/W (IO52) and extended R/W (IO53) commands
- Supports Read Wait Control, Suspend/Resume operations
- Supports multiple slots/cards
- Injection and detection of error conditions such as CRC, timeout, invalid commands, and protocol errors
- User-friendly monitor
- Supports MMC specification version 3.31 and version 4.3
- Supports CE-ATA Digital Protocol revision 1.1RC

Overview

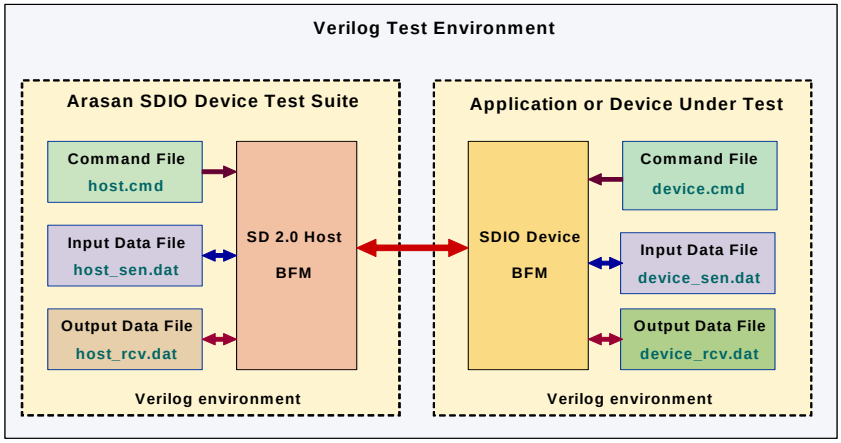
The Arasan SD/SDIO Host/Device Verification IP is a comprehensive test environment for verification, validation, debugging, and testing of SD Host and SDIO device applications for functionality, compliance, or interoperability. The SD/SDIO Verification IP allows the complete and extensive testing of an SD Host or SDIO device application, it also ensures full functionality of the SoC or ASIC before the design is finalized. The SD/SDIO Verification IP is delivered with a interconnected host and device test environment, the same setup supports the verification and testing of SD/SDIO/MMC/CE-ATA device IPs as well as SD/SDIO/MMC/CE-ATA host IPs.

The Arasan SD/SDIO Host/Device Verification IP consists of the SD 2.0 Host controller behavior functional model (BFM), SD 2.0 Device controller behavior functional model (BFM), Command Files, Input Data Files, Output Data Files, and Monitor (diagram next page). The Command File provides a comprehensive set of test vectors as well as a complete set of SD 2.0/SDIO 2.0 compliant commands for extensive testing. The verification IP is an RTL design in Verilog. A Verilog test environment can be setup easily by replacing the SD Host or SDIO Device IP of the Arasan SD/SDIO Verification IP with the application IP or device under test (DUT), no interconnection on the SD bus is required.

With the verification IP, many of the time consuming simulations such as timeout can be shorten significantly. The SD/SDIO Host/Device Verification IP also allows the injection and detection of errors and exception conditions. These error conditions include CRC, timeout, invalid commands, and protocol errors.

The Arasan SD Host BFM also supports multiple cards, SD1, SD4, SPI, high-speed, and full-speed transfer modes, MMC 1/4/8-bit modes, and CE-ATA 1/4/8-bit modes.

SD/SDIO Verification IP in a Test Environment with SDIO Device DUT.



Version 1.0a

SD 2.0 Compliant
SDIO 2.0 Compliant

MMC 4.3 compliant

CE-ATA 1.1 compliant

SD/SDIO Host/Device Verification IP

SD 2.0 Host/SDIO 2.0 BFM:

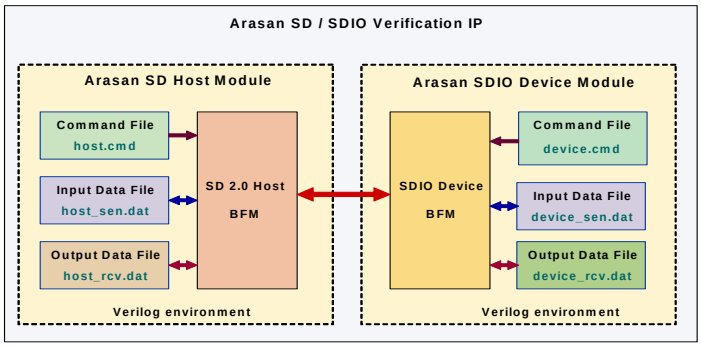
The SD Host BFM consists of the behavior models of the SD 2.0 host controller and DMA controller. The Bus Interface Unit (BIU) consists of the Command Decoder, Response Generator, Transmitter/Receiver, and Power Control/Switch units. SD1, SD4, and SPI modes are supported. Other BIU functions includes the 16-bit CRC generator and checker for the data lines, 7-bit CRC generator and checker for the command and response lines, interrupt state machine, and BIU master state machine. The MMC and CE-ATA Host models are also included.

The SDIO Device houses the 16 bit CRC generator and checker for the data lines, 7 bit CRC generator and checker for the command and response lines, transmitter state machine, receiver state machine, interrupt state machine, BIU master state machine, command decoder, and response generator. The BIU bus capability is determined by the bit values programmed in the R/W CCCR registers.

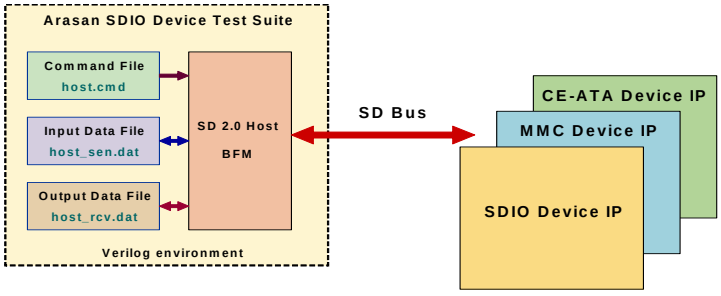
Command, Input and Output Files:

Other components of the SDIO Device Verification IP includes the Command File, Input Data File, and Output Data File. The Command File consists of a list of SD/SDIO commands and test cases. The Command File provides inputs to the SD Host Controller BFM for configuration, functions initiation, testing, and debugging. The test environment also supports users defined data / command generation as well as error injection. The Input Data File provides input data to the SD host BFM and the Output Data File records data sent out from the SD Host BFM. Similar files are provided on the SDIO side to provide similar functions.

Arasan SD/SDIO Host/Device Verification IP functional block diagram.



SDIO Device Verification IP supports SDIO, MMC, and CE-ATA device IPs.



Benefits:

- Fully compliant test environment
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- Verilog RTL source test bench
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

SD/SDIO Host/Device Verification IP:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com