

Features

- Support Verilog test environment
- Functional verification, validation, and compliance testing of SoC or ASIC designs
- MIPI compliant DSI Host BFM, DSI Device BFM, and D-PHY BFM
- Compliant to MIPI DSI Specification Version 1.02, Display Pixel Interface (DPI-2) Version 2.00, Display Bus Interface (DBI-2) version 2.00, and Display Command Set version 1.00a
- Compliant to MIPI DSI Display Serial Interface (Version 1.01.00)
- Complaint to MIPI D-PHY Version 0.81
- Supports type 1, 2, 3, and 4 display architectures for command and video modes
- DSI host supports two virtual channels
- DSI device supports four virtual channels
- One to four PHY data lanes
- Supports command and video modes
- Supports 16bpp RGB565, 18bpp RGB666, and 24bpp RGB888 pixel formats
- Contention recovery mechanism
- Supports QQVGA, OCIF, QVGA, CIF, VGA, WVGA, and XVGA (host)
- Supports burst mode for one video channel and non-burst mode for dual channel
- Supports VGA 616 x 480 and WVGA 800 x 480 resolutions (device)
- One DPI for pixel stream transfer (host and device)
- One DBI for pixel stream and command transfers (host)
- Switching to ultra low power mode during shutdown
- Recovery schemes for fault errors
- Supports bus turnaround
- Interfaces to MIPI compliant D-PHY transceivers
- Injection and detection of error conditions for DSI host, device, and D-PHY

DSI Verification IP

Overview

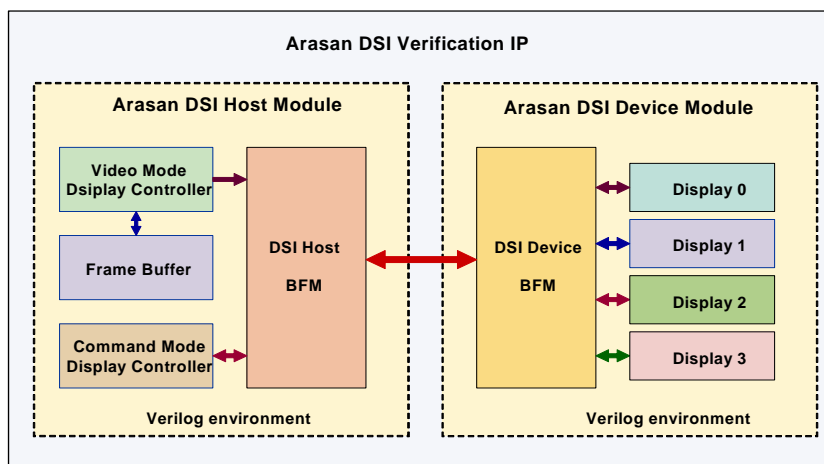
The Arasan DSI Verification IP is a comprehensive test environment for verification, validation, debugging, and testing of MIPI DSI (Display Serial Interface) applications for functionality, compliance, or interoperability. The DSI Verification IP allows the complete and extensive testing of DSI applications, it also ensures full functionality of the SoC or ASIC before the design is finalized. The MIPI compliant DSI Verification IP is delivered with an interconnected host and device test environment, the same setup supports the verification and testing of MIPI DSI device IPs as well as MIPI DSI host IPs.

The Arasan DSI Verification IP includes a DSI Host module, a DSI Device module, and a D-PHY module. The DSI Host module consists of the DSI Host controller behavior functional model (BFM), Command File, Input Data File, Output Data File, and Monitor. The Command File provides a comprehensive set of test vectors as well as a complete set of MIPI DSI compliant commands for extensive testing. The verification IP is an RTL design in Verilog. A Verilog test environment can be setup easily by replacing the DSI IP of the DSI Verification IP with the application IP or device under test (DUT), no interconnection on the DSI bus is required. The DSI Device module consists of components similar to that of the DSI Host module. For applications written in VHDL, a mixed test environment can be employed.

With the verification IP, many of the time consuming simulations such as time-out can be shorten significantly. The DSI Verification IP also allows the injection and detection of errors and exception conditions. These error conditions include CRC, ECC, time-out, invalid commands, and protocol errors.

The DSI Verification IP supports video mode, command mode, major pixel formats, burst mode, non-burst mode, virtual channels, DPI, and DBI.

Arasan DSI Verification IP



DSI Verification IP

DSI Host BFM:

The DSI Host BFM consists of the DSI protocol layer and PPI_PHY layer. The DSI protocol layer is responsible for the DSI specific functionality, and the PHY layer is responsible for the PHY functionality. The DSI host model reads commands from a command file. Based on the tasks listed in the command file, pixel data is generated from the respective data files. If the command is of the type "long packet", each long packet will consist of a packet header along with the supplied parameters like word count, data identifier, virtual channel number, ECC, payload data, and CRC.

Since both layers are supported, PHY layer commands can be issued to change the DSI controller operating mode to ultra low power mode, low power mode, or bus turnaround.

DSI Device BFM:

The DSI Device BFM handles the DSI receiver protocol and PHY specific protocol. De-packetization is carried out by

this model based on the accompanied packet headers or data identifier types. Received payload data is sent to respective data collector files. The packet reception sequence is listed in a packet data file. Based on the specified virtual channel, the packet is routed to different display panel. Trigger messages, short packets or long packets can also be sent by the receiver during bus turnaround. Data needed to be packed at low power mode is fetched from a data sending file. Contention on the DSI traffic can also be forced using this model.

PHY Receiver Model:

The D-PHY model emulates the functionality of a D-PHY transceiver. The model drives the differential signals at high-speed during transmission. It combines the multi-lane signals into a single stream during reception. This D-PHY model also handles low power single ended signals during reception and transmission.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Customer training available
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog



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Arasan Chip Systems, Inc.

1150 N. First St. Suite #201
San Jose CA 95112
Phone: 408-282-1600
Fax: 408-282-7800
E-mail: sales@arasan.com

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