

AC5000 SDIO Host Controller ASSP

Features

- Meets SD Host Controller Standard Specification Version 2.00
- Meets SDIO Card Specification version 2.0
- Meets SD Memory Card Security Specification version 1.10
- Meets MMC Specification version 3.31, 4.1, and 4.2
- Meets CE-ATA Digital Protocol revision 1.1RC
- Supports CE-ATA Digital Protocol commands (CMD60 / CMD61)
- Supports MMC Plus and MMC Mobile
- Card detection (insertion/removal)
- Supports 1-bit SD, 4-bit SD, and 8-bit MMC modes
- Supports 4 slots (2 CE-ATA/MMC4 8-bit slots and 2 SD/SDIO 4-bit slots)
- All cards work simultaneously with different clock speeds
- Card interrupt to host is allowed in 1 and 4-bit SD modes
- Up to 200 Mbit/sec and 416 Mbit/sec read/write data rates with 4 and 8 parallel data lines respectively
- CRC7 and CRC16 for data integrity
- ECC support for MMC4.0 cards
- Works with I/O cards, read-only cards and read/write cards
- Supports FIFO overrun and underrun conditions by stopping SD clock
- Supports synchronous/asynchronous microprocessor interface
- DMA and interrupt transfer modes
- 8/16 bit microprocessor data bus
- Supports Intel XScale and OMAP5910 microprocessor interfaces
- Supports standard SRAM, VLIO, and EBI interfaces

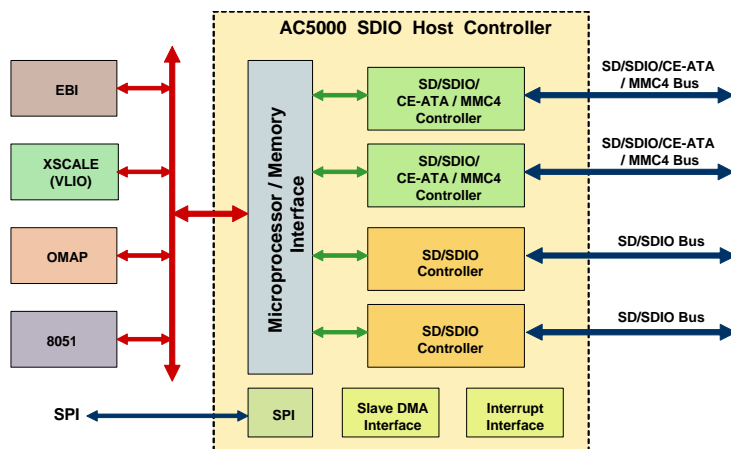
Overview

Connecting to microprocessor / memory interface, the AC5000 expand the capability of your mobile applications by offering 2 SD/SDIO/MMC4.1/CE-ATA ports and 2 SD/SD host ports with high throughput. The AC5000 meets many mobile design requirements when power and pin count are limited. The AC5000 Host Controller consists of the SD Host 2.00, SDIO 2.0, SD Memory 1.10, MMC 3.31/4.1/4.2, and CE-ATA 1.1RC, and microprocessor/memory interfaces.

The SD, SDIO, MMC, and CE-ATA protocols are handled by AC5000 at transmission level. These include packing data, adding Cyclic Redundancy Check (CRC), setting of Start/End bit, and checking of transaction format correctness. The AC5000 supports two CE-ATA/MMC4 8-bit slot and two SD/SDIO 4-bit slots. Each slot is controlled independently and can be accessed simultaneously. This enables support for combinations of full-speed and low-speed cards under different SD clock frequencies. The CE-ATA controller provides an optimized HDD Interface for handhelds. The CE-ATA interface utilizes the same MMC command sequences for initialization and new commands (CMD60 & CMD61) defined by CE-ATA for efficient HDD command execution.

AC5000 provides logic to transfer data from the system memory to the SD/SDIO/MMC4/CE-ATA data bus. This block also contains a bus monitor which monitors the bus activity and check for any timing violations. The microprocessor interface supports programmed IO and DMA data transfer methods. In programmed IO method, the CPU transfer data using the Buffer Data Port register. The synchronous/asynchronous 8/16 bit data bus microprocessor/memory bus supports SRAM interface, EBI, VLIO, Intel XScale, TI OMAP5910, and 8051.

AC5000 SDIO Host Controller ASSP interfacing to external buses



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SD/SDIO/MMC4/CE-ATA Interfaces:

The SD/SDIO interface communicates with the SD host through the SD bus. SD1, SD4 and SPI transfer modes are supported. The SD/SDIO interface houses the 16 bit CRC generator and checker for the data lines, 7 bit CRC generator and checker for the command and response lines, transmitter state machine, receiver state machine, interrupt state machine, SD/SDIO interface master state machine, command decoder, and response generator. The SD/SDIO interface bus capability is determined by bit values programmed in the R/W CCCR registers. At reset, the SD bus is set to SD 1-bit mode.

The MMC interface conforms with version 3.31 and version 4.1 specifications. It supports 8-bit MMC mode, Error Correction Code (ECC), MMCplus, and MMCmobile card types.

The CE-ATA Host Controller interface conforms to CE-ATA Digital Protocol revision 1.1RC, with support for CE-ATA Digital Protocol commands (CMD60 / CMD61). The CE-ATA interface allows for lower pin count, better power utilization, voltages tailored to battery-based applications, and more efficient command protocol.

Microprocessor Interface:

The microprocessor interface supports programmed IO and DMA data transfer methods. In programmed IO method, the CPU transfer data using the Buffer Data Port register. The processor bus interface supports most popular processors for mobile applications. These

include processors from Intel (XScale), TI (OMAP5910), Qualcomm, and Samsung. The interface also supports 8051 processor that interfaces to the AC5000 for medical, automotive, and other consumer electronics applications. The microprocessor bus also supports interrupt transfer mode.

VLIO Interface:

The Variable Latency I/O (VLIO) interface only requires a small number of additional components and produces low-cost and efficient Direct Memory Access performance. The Microprocessor/Memory interface supports devices with a VLIO interface.

EBI Interface:

The External Bus Interface (EBI) enables several memory controllers to share the same external address and data pins. By sharing pins, the pin count and final package size of the device is reduced while providing access and control of external memories. The Microprocessor/Memory interface supports devices with an EBI interface.

Custom Design Services:

Arasan Chip Systems is experienced in providing custom design services including logic, SoC, system and software designs.

Supported OS for Device Drivers:

WinXP, and, Linux.

Benefits:

- All interfaces fully compliance to latest standards
- Premier direct support from Arasan IP core designers
- Hardware Evaluation Kit is available
- Client drivers for Source codes for Virtual serial drivers
- Customer training available



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Arasan Chip Systems, Inc.

1150 N. First St. Suite #201
San Jose CA 95112
Phone: 408-282-1600
Fax: 408-282-7800

Data Sheet Links:

AC5000 SDIO Host Controller:
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