

Features

General Functions:

- Full-duplex and half-duplex modes of operation
- Supports IEEE 802.3-2002 compliant MII
- Optional support for RMII, and SMII to reduce pin counts
- Independent 32-bit scatter-gather DMA with big/little endian operation
- Optional VLAN Q-Tag frame support
- CSMA/CD Protocol for half-duplex mode
- PAUSE frame based flow control in full-duplex mode
- MDIO/MDC management interface
- 802.3 compliant MIB, SNMP, RMON management support
- Configurable transmit and receive FIFOs
- Supports Jumbo frames
- Support magic packet and Wake-Up frames
- Optional AXI, AHB, PCIe, PCI, or custom bus interface

Transmit Functions:

- Variable length Inter Frame Gap (IFG) on back to back frame transmission
- Variable length (3, 5, 7 bytes) preamble generation
- Automatic generation of FCS and PAD
- Option to disable PAD or CRC32
- Auto retransmission on collisions in half-duplex

Receive Functions:

- Inter Frame Gap checking
- Preamble detection and stripping
- Flexible address filtering modes and inverse address filtering
- 64-bit hash table to filter multicast addresses
- Promiscuous mode of operation
- Reception of broadcast frames
- Automatic checking the FCS field, runt frames, and data field length
- Detection of MaxFrameLen frames, receive errors
- 32-bit status information on each receive frame

Flow Control Functions:

- Software controlled PAUSE control frame generation including multicast and unicast address.
- Automatic detection and checking of PAUSE frames
- Option to block PAUSE frames

10/100 Ethernet IP

Overview

The Arasan 10/100 Ethernet Media Access Controller IP is compliant with the Ethernet IEEE 802.3-2002 standard and has passed inter-operability testing at UNH-IOL. The 10/100 Ethernet IP provides an 10/100 Mbps Media Independent Interface (MII) and an optional processor interface; it also supports Reduced MII (RMII) and Serial MII (SMII). The 10/100 Ethernet IP is designed for SoC and mobile applications such as integrated networking devices, PCI-Express Ethernet controllers, and Ethernet adapter cards.

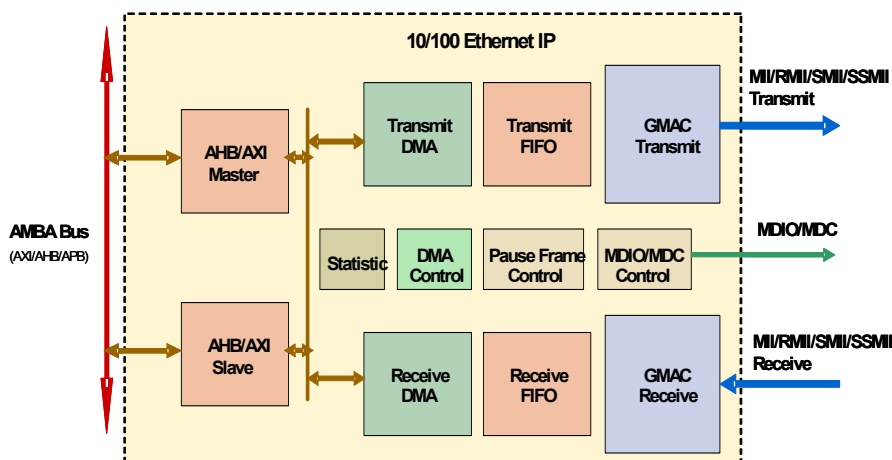
The 10/100 Ethernet IP supports half-duplex mode at 10/100 Mbps and full-duplex mode at 10/100 Mbps. The IP core consists of two configurable FIFOs on both transmit and receive sides to handle the application's latency during frame transmission and reception. An available 32-bit scatter-gather DMA transfer packets between the internal FIFOs and the host memory to enhance system performance.

The IP core supports 4-bit MII based 10/100 Mbps PHY. IA MDIO/MDC (Management Data Input/Output and Management Data Clock) management interface provides controlling and management functions to external PHY devices.

The 10/100 Ethernet IP provides enhanced programmable features for minimizing applications complexity and pre/post message processing. These features support MIB, SNMP, RMON, VLAN Q-Tag frame, and Jumbo frames. It also includes dynamic generation, checking, and stripping of FCS field, automatic pad field insertion, automatic retransmission and detection of collision frames, collision avoidance and handling. Other features are generation and decoding of PAUSE control frames, frame boundary delimitation, frame synchronization, and error detection.

The 10/100 Ethernet IP is an RTL design in Verilog that implements an Ethernet controller on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications.

10/100 Ethernet Controller IP Functional Block Diagram.



10/100 Ethernet IP

MII/RMII/SMII Interface:

The MII interface is compliant to the IEEE 802.3-2002 clause 22. The interfaces can be connected to any standard compliant MII PHY. The RMII is an optional 2-bit interface for reduce pin count and achieve the same functionality as the MII interface. The IP core also supports SMII as optional interface. Both Full-duplex mode and half-duplex mode are supported.

10/100 Ethernet Receiver:

The receiver can be programmed to check minimum Inter Frame Gap (IFG) between frames and handles minimum IFG of 64 BT during back to back frame reception. It can also handles reception of frames with no preamble and only SFD. The receiver implement flexible address filtering mode with four 48-bit MAC addresses. A 64-bit hash table is included to filter multicast addresses.

10/100 Ethernet Transmitter:

The transmitter supports variable length (64 BT, 96 BT, 128 BT, 256 BT) IFG on back to back frame transmission with default value of 128 bit times of IFG. It also supports variable length (3, 5, 7 bytes) preamble generation with default of 7 bytes of preamble. Other features include automatic generation of FCS and PAD during transmission, option to disable PAD and/or CRC32 insertion on transmission on a per frame basis, and option to shield the application for frame retransmission process on collisions during half-duplex mode.

Related Products

Arasan has a software driver for the Fast (10/100 Mbps) Ethernet IP for Windows and Linux OS. To accelerate system design, an Ethernet Hardware Development Kit is available. Arasan also has a Gigabit (10/100/1000 Mbps) Ethernet IP core and corresponding driver.

MDIO/MDC Interface:

The MDIO/MDC interface is a 2-wire interface used to configure and control external IEEE802.3 compliant PHY devices using the MII Management Frame structure. The interface is defined in the IEEE802.3 Specification.

DMA:

The 32-bit scatter-gather DMA supports either the linked-list or ring (chained) descriptors. The skip length is programmable between descriptors when chained descriptors are used. Up to two buffers per descriptor are supported. The transmit DMA and receive DMA are operating independently. A programmable interrupt structure is used for the DMA. Big or little endian operation is supported.

Host Interface:

Available host interfaces for the 10/100 Ethernet IP include AXI, AHB, PCIe, PCI, and custom interfaces. The bus master interface is used to transfer packets between the host memory and the internal FIFOs. The slave interface is used to control the operation of the Ethernet controller and to program the registers inside the core.

Custom Interface:

The 10/100 Ethernet IP core also supports PowerPC, MIPS, SH3/SH4, 8051, and other processor buses. In addition, standard interfaces like PCI and PCIe, and custom bus interface with special requirements can also be implemented.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Un-encrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

Related Products:

- Ethernet Windows / Linux Driver
- Gigabit Ethernet IP
- Ethernet Hardware Development Kit (HDK)

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Data Sheet Links:

10/100 Ethernet IP:
<http://www.arasan.com/datasheets/login.php>

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