

# USB 2.0 OTG IP Core

## Features

- **USB 2.0 Compliance**
  - OTG Supplement Rev. 1.0a
  - High speed support: 480 Mbit/s
  - Full speed support: 12 Mbit/s
  - Low speed support: 1.5 Mbit/s
- **USB Interface**
  - Standard USB 2.0 transceiver interface: 8/16 bit UTMI/ULPI interface
  - Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - Supports data-line pulsing and Vbus pulsing as A-device or B-device
- **Endpoint Configuration**
  - Configurable up to 15 Tx and Rx endpoints
  - Configuration options
    - Bulk, control, isochronous, interrupt
  - Dedicated control endpoint zero
- **RAM Configuration**
  - Configurable dual port RAM shared between endpoints
  - Separate RAMs for upstream and downstream traffic
- **Power Management Support**
  - Suspend/resume support for power management
- **System Bus Interface**
  - Direct addressing of all IP core registers from PCI, AHB, or Custom bus

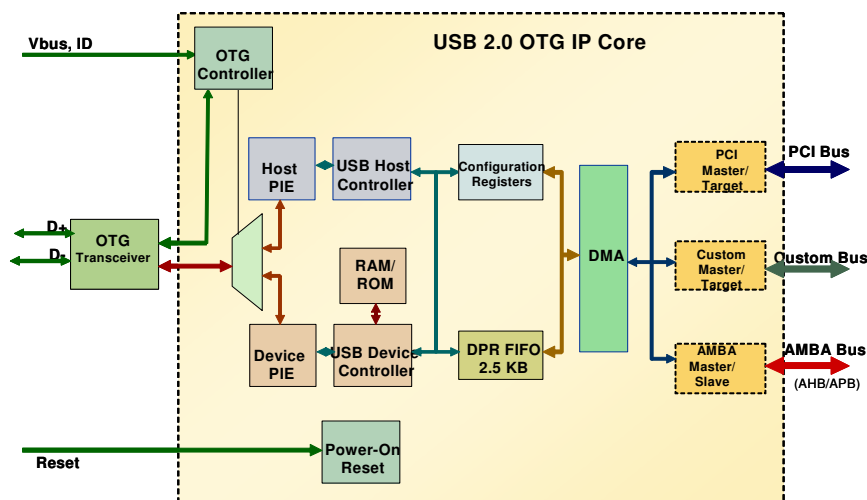
## Overview

The Arasan USB 2.0 OTG IP Core is compliant with the OTG Supplement Rev. 1.0a. The USB 2.0 OTG core supports both Host Controller, Device Controller and OTG functionality. When operating as a host (A-device), it supports 480 Mbit/s in High Speed (HS) mode, 12 Mbit/s in Full Speed (FS) mode, and 1.5 Mbit/s in Low Speed (LS) mode. When operating as a peripheral (B-device), it supports HS and FS modes.

Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) are managed by the SRP/HNP Control Logic. SRP allows a B-device to request an A-device to turn on Vbus to start a session. HNP allows two connected dual-role devices to change roles and eliminates the needs for the user to switch cable connections. The Vbus Control Circuit supports: a) the generation of data-line pulsing and Vbus pulsing methods when initiating the SRP as a B-device, b) the detection of both pulsing methods when acting as an A-device, and c) the sourcing of a minimum of 8 mA on Vbus. The Vbus Control Circuit also handles the pull-up and pull-down connections to D+ and D- during host/device role switching. The SRP/HNP Logic and Vbus Control Circuit control the operating mode of an USB port as either a host or peripheral. The Arasan USB 2.0 OTG port requires an external USB 2.0 transceiver with a standard UTMI interface.

The Arasan USB 2.0 OTG IP Core offers a high level of flexibility, allowing designers to implement the USB 2.0 OTG port with a wide selection of processor interfaces. AHB, PCI, and Custom buses are available to provide a high-speed connection to the USB interface. The Arasan USB 2.0 OTG IP Core is augmented by the availability of the Arasan OTG Software Stack that supports host driver, device driver, class of devices, and Linux operating system. The Arasan USB 2.0 OTG IP Core is an RTL design in Verilog that implements an USB 2.0 OTG controller for an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for full verification.

USB 2.0 OTG IP Core Functional Block Diagram



# USB 2.0 OTG IP Core

## OTG Controller:

The Vbus Control Circuit controls and monitors the voltage levels of Vbus, D+, and D- during SRP and HNP transactions. The SRP/HNP Logic of the OTG Controller consists of state machines that perform the SRP and HNP protocols as well as the configuration of an OTG port as a host or device. OTG descriptors are provided in the SRP/HNP Logic during enumeration.

## Dual Role USB Core:

Each dual-role core consists of an USB 2.0 compliant host controller and an USB 2.0 compliant

device controller. The SRP/HNP Logic in the OTG Controller determines the role of a dual-role core depending on the setting of the ID pin or the result of HNP.

## System Bus Interface:

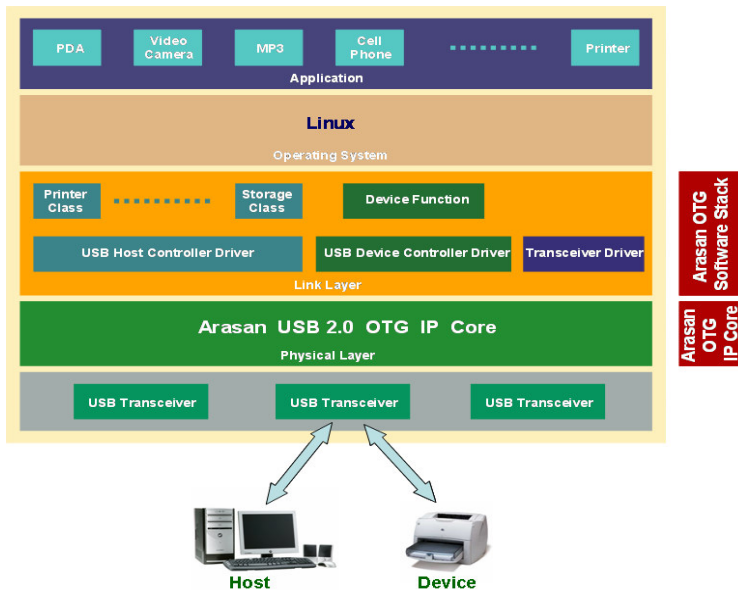
The Arasan OTG Core can support AXI, AHB or OCP as the standard interfaces. The OTG core can be optimized to support any custom bus interfaces with the flexible architecture.

## Benefits:

- Complete hardware and software OTG solution
- Fully compliant USB 2.0 OTG IP Core
- Premier direct support from Arasan IP core designers

## Deliverables:

- USB 2.0 OTG core with synthesizable Verilog RTL
- Synthesis scripts
- Test environment and test case database
- Configuration utility



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