

## SDIO Device IP Core

### Features

- Meets SDIO v2.0 Specification Part E1
- Up to 7 functions in SPI, SD1, and SD4 mode
- Host clock rate from 0 to 50 MHz
- Supports SPI, 1-bit, and 4-bit SD modes
- Supports miniSDIO
- Embedded SDIO ATA standard function interface code
- SDIO combo mode
- Extended 2.7 – 3.6V operating voltage
- Hardware interrupt to host
- Maximum 200 Mbit/s read/write with 4-bit data lines in SD4 mode
- CRC7 and CRC16 modules
- Supports commands including direct R/W (IO52) and extended R/W (IO53)
- Supports Read Wait Control, Suspend/Resume operations
- Programmable through AMBA 2.0 AHB bus

### Optional Bus Interfaces

- 300 MHz 32-bit AHB bus
- Avalon interface
- BVCI interface
- Parallel interface
- SPI master/slave interface

### Overview

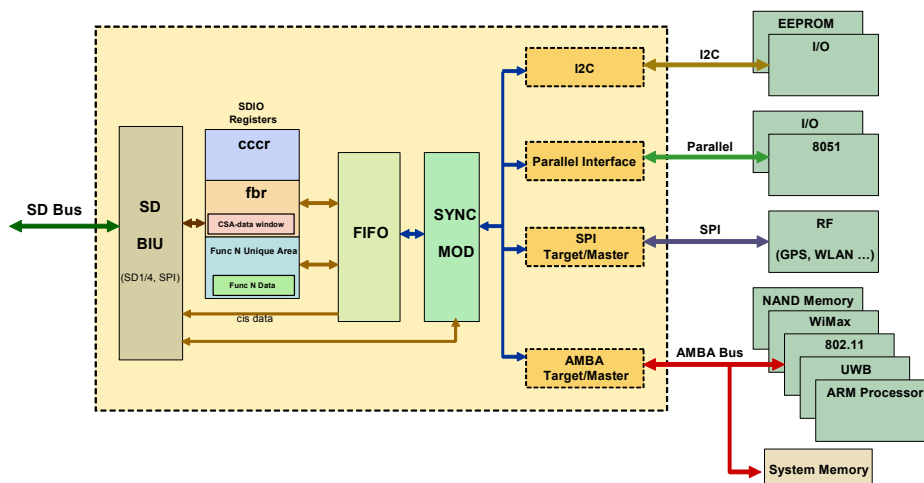
The Arasan SDIO Device IP core (SDIO Card Controller IP core) controls the communication between devices connected to the SD/SDIO bus and devices connected to the local bus. The flexible architecture of the Arasan SDIO Device IP core allows the support of a wide range of portable low-power applications such as the 802.11 devices, GPS, WiMAX, UWB, etc.

The SDIO Device IP core is fully compliant with the SDIO Specification version 2.0 Part E1. It supports SPI, SD1, and SD4 bit transfer modes, and 7 functions per card. High-speed and full-speed SD data transfers are also supported. Other supported version 2.0 features are SDHC, SDHS, miniSDIO, embedded SDIO ATA standard function interface code, and extended 2.7 - 3.6V operating voltage. In applications with an AHB interface, the Arasan SDIO Device IP core interfaces with the ARM processor at a clock speed up to 300 MHz. The SDIO Device controller includes an internal FIFO that is expandable from a minimum size of 4 x 32-bit to a size required by the application.

Virtually all major interfaces are supported by the Arasan SDIO Device IP core. These include the Avalon, BVCI, parallel, SPI, and custom specific buses. The wide selection of interfaces available enables the SDIO Card Controller IP core to be integrated effectively in most of the complex SOC and SOPC designs today.

The SDIO Device IP core is an RTL design in Verilog that implements an SDIO device controller on an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for verification. The Arasan SDIO Device IP core has been widely used in different SDIO applications by major chip vendors with proven silicon.

SDIO Device IP Core Functional Block Diagram



# SDIO Device IP Core

## Bus Interface Unit (BIU):

The BIU communicates with the SD host through the SD bus. SD1, SD4, and SPI transfer modes are supported. The BIU houses the 16 bit CRC generator and checker for the data lines, 7 bit CRC generator and checker for the command and response lines, transmitter state machine, receiver state machine, interrupt state machine, BIU master state machine, command decoder, and the response generator. The BIU bus capability is determined by bit values programmed in the R/W CCCR registers.

## AHB/APB Interface:

This AHB/APB Master is responsible for transferring data between the ARM Processor and Arasan SDIO-AHB/APB bridge for read and write operations. The AHB/APB slave block consists of the Operational registers. Reading and writing of these registers are handled by the Arasan SDIO-AHB/APB bridge or Arm processor. The ARM processor sets the io\_ready bit in the program register when it is ready to operate, indicating to the SD host that all initialization has been done and function is ready to operate.

## Parallel Interface:

A slave or I/O device can be connected to the optional parallel bus interface. Behavior of the I/O is controlled by the SD host. A data communication channel can also be established between the SD bus and an 8051 embedded system through the parallel bus interface. The parallel bus interface supports 8-bit or 16-bit mode with a maximum throughput of 10 Mbyte/sec.

## Avalon Interface:

Combining peripherals, bus masters or processors with different interface standards together in a SOC

design is a big challenge. The Avalon specification defines a switch fabric that allows any type of processor or bus master to be connected to any type of peripheral. Implementing SOPC (Silicon On Programmable Chip) on an FPGA is simplified by using software tools to create the interconnect strategy that optimizes the performance of the attached Avalon devices. The Arasan SDIO Device - Avalon Master IP provides all the glue logic that enables the direct connection of a SDIO device to an Avalon based SOPC system.

## BVCI Interface:

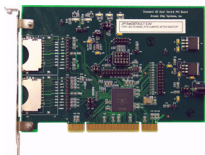
Virtual Component Interface Standard specifies a kind of standardized point-to-point interface for connecting SoC IP-blocks together in a common and reusable manner. The VCI standard facilitates communication between virtual components, possibly those created by separate design sources. The Arasan SDIO Device IP core with BVCI interface consists of the SDIO version 2.0 and BVCI (Basic Virtual Component Interface) interface. The IP is suitable for low power memory or I/O card applications such as WLAN and Bluetooth.

## SPI Interface:

Application such as a GPS or RF device requires the conversion of SPI data format to SD data format. The Arasan SDIO Device IP core is designed to handle such functions at high speed. The SPI supports maximum clock rate of 25 MHz.

## Device Hardware Validation Platform (HVP):

The HVP is a PCI plug-in card for validation and compliance testing of SDIO devices .



## Device Hardware Development Kit (HDK):

The HDK is designed for SDIO device prototyping and driver development.



## Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Optional Items:

- Device Hardware Development Kit (HDK)
- Device Hardware Validation Platform (HVP)
- SDIO Linux stack

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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## Data Sheet Links:

SDIO Device IP with AHB, Avalon, or BVCI interface:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)

