

## SDIO 3.0 Device IP Core

### Features

- Compliant with SD Specification Part E1 SDIO Specification 3.0
- Supports Asynchronous Interrupt to Host controller
- Enhanced power management using new Power State Control function
- Supports Read Wait Control, Suspend/Resume operations for superior card performance
- High-performance cards UHS-I (104MB/s)
- Multiple I/O functions and one memory supported
- Host clock rate from 0 to 208 MHz
- Supports SPI, 1-bit, and 4-bit SD modes. Optional 8-bit mode for embedded SDIO
- All SDIO form factors supported - standard, mini and micro SDIO card
- Embedded SDIO ATA standard function interface code
- Bus Master with Scatter Gather DMA
- Dual operating voltage range 2.7V – 3.6V and 1.7V - 1.95V
- Maximum 104 MB/s read/write with 4-bit data lines in SD4 mode
- CRC7 for command and CRC16 for data integrity - optional in SPI mode
- Supports commands including direct R/W (IO52) and extended R/W (IO53)
- Programmable through AMBA 3.0 AHB bus

### Optional Bus Interfaces

- AXI interface
- OCP interface
- Avalon interface
- BVIC interface
- Custom interface
- SPI master/slave interface

### Overview

The SDIO 3.0 Device IP core is used to implement SDIO cards that are connected to a Host processor over a standard SD bus. The flexible architecture of the SDIO Device IP core is targeted to develop a range of portable, low-power cards such as the WiFi (802.11), GPS, WiMAX, UWB, LTE.

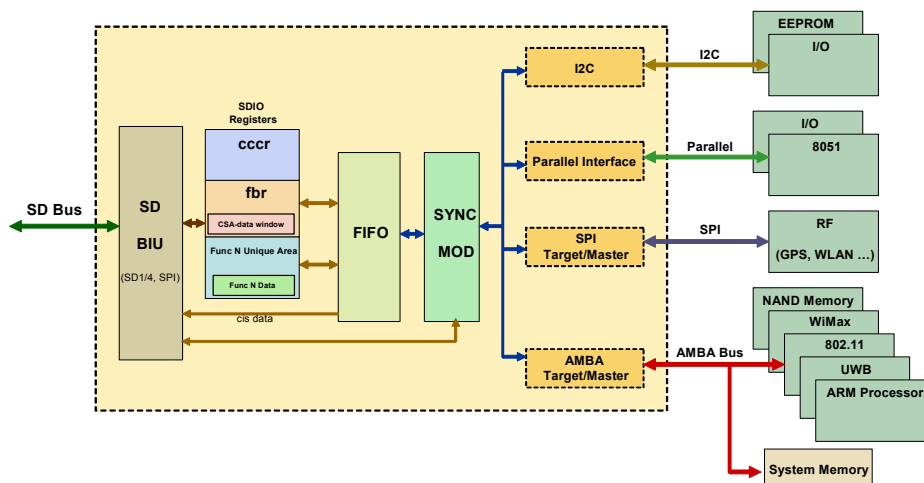
The SDIO 3.0 Device IP core is fully compliant with the SD Specification Part E1 SDIO 3.0. It supports SPI, SD1, and SD4 bit transfer modes, and multiple functions per card. High-speed and full-speed SD data transfers are also supported. All version 3.0 features supported such as UHS-I, SDHS, miniSDIO, embedded SDIO ATA standard function interface code, and extended 2.7 - 3.6V operating voltage. In applications with an AHB interface, the SDIO Device IP core interfaces with the ARM processor. The SDIO Device controller includes an internal FIFO that is expandable from a minimum size of 4 x 32-bit to a size required by the application.

The IP supports asynchronous interrupts to the Host processor for improved performance. In addition it supports suspend, resume operation that benefits high-performance multi-function cards. The controller integrates a scatter gather DMA engine which reduces the CPU overhead for data transfers between a SDIO card and system memory.

Virtually all major interfaces are supported by the SDIO Device IP core. These include the AHB, AXI, OCP, Avalon, BVIC, SPI and custom specific buses. The wide selection of interfaces available enables the SDIO Card Controller IP core to be integrated effectively even in the most of the complex SOC designs today.

Arasan offers a Total IP Solution for its SDIO 3.0 Device IP consisting of RTL source files, synthesis scripts, test environment which are backed by our World-class customer support.

SDIO 3.0 Device IP Core Functional Block Diagram



# SDIO 3.0 Device IP Core

## Bus Interface Unit (BIU):

The BIU communicates with the SD host through the SD bus. SD1, SD4, and SPI transfer modes are supported. The BIU houses the 16 bit CRC generator and checker for the data lines, 7 bit CRC generator and checker for the command and response lines, transmitter state machine, receiver state machine, interrupt state machine, BIU master state machine, command decoder, and the response generator. The BIU bus capability is determined by bit values programmed in the R/W CCCR registers.

## AHB/APB Interface:

This AHB/APB Master is responsible for transferring data between the ARM Processor and the SDIO-AHB/APB bridge for read and write operations using Scatter Gather DMA. The AHB/APB slave block consists of the Operational registers. Reading and writing of these registers are handled by the SDIO-AHB/APB bridge or ARM processor. The ARM processor sets the io\_ready bit in the program register when it is ready to operate, indicating to the SD host that all initialization has been done and function is ready to operate.

## Parallel Interface:

A slave or I/O device can be connected to the optional parallel bus interface. Behavior of the I/O is controlled by the SD host. A data communication channel can also be established between the SD bus and an 8051 embedded system through the parallel bus interface. The parallel bus interface supports 8-bit or 16-bit mode.

## Avalon Interface:

Combining peripherals, bus masters or processors with different interface standards together in a SOC design is a big challenge. The Avalon specification

defines a switch fabric that allows any type of processor or bus master to be connected to any type of peripheral. Implementing SOPC (Silicon On Programmable Chip) on an FPGA is simplified by using software tools to create the interconnect strategy that optimizes the performance of the attached Avalon devices. The SDIO Device - Avalon Master IP provides all the glue logic that enables the direct connection of a SDIO device to an Avalon based SOPC system.

## BVCI Interface:

Virtual Component Interface Standard specifies a kind of standardized point-to-point interface for connecting SoC IP-blocks together in a common and reusable manner. The VCI standard facilitates communication between virtual components, possibly those created by separate design sources. The SDIO Device IP core with BVCI interface consists of the SDIO version 3.0 and BVCI (Basic Virtual Component Interface) interface. The IP is suitable for low power memory or I/O card applications such as WLAN and Bluetooth.

## SPI Interface:

Application such as a GPS or RF device requires the conversion of SPI data format to SD data format. The SDIO Device IP core is designed to handle such functions at high speed. The SPI supports maximum clock rate of 25 MHz.

## Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Optional Items:

- SDIO Linux Host stack

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

## Arasan Chip Systems, Inc.

2010 N. First St. Suite #510  
San Jose CA 95131  
Phone: 408-282-1600  
Fax: 408-282-7800  
E-mail: sales@arasan.com

## Data Sheet Links:

SDIO 3.0 Device IP:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)

