

SD/MMC/CE-ATA Host IP

Features

SD / SDIO:

- Meets SD Host Controller specification Version 2.0 Part A2
- Meets SDIO card v2.0 specification
- Supports Embedded SDIO Specification Version 0.92 Draft
- Up to 7 functions in SPI, SD1, or SD4 mode
- Up to 200 Mbit/s with 4 parallel SD data lines
- Supports Test Register to generate events by software
- Supports high capacity Ver2.00 Card
- CRC7 and CRC16 modules
- Supports direct R/W (IO52) and extended R/W (IO53) commands
- Supports Read Wait Control, Suspend/Resume operations

MMC / eMMC

- Meets MMC specifications 3.31, 4.1, 4.2, and eMMC (4.3)
- Supports MMCplus, MMCmobile
- 416 Mbit/s with 8 parallel MMC 4.2 data lines
- Supports MMC 8-bit mode
- Power-on boot mode
- Sector address allows host to access high capacity card
- Sleep mode for power saving
- CID register to recognize eMMC or card

CE-ATA

- Meets CE-ATA Digital Protocol revision 1.1RC
- Supports CE-ATA 8-bit mode
- Supports CE-ATA Digital Protocol commands (CMD39/CMD60/CMD61)

System Architecture

- Supports non-DMA, SDMA, ADMA1, and ADMA2 modes
- Host clock rate from 0 to 52 MHz
- Optional 300 MHz 32-bit AHB bus
- Optional PCI specification 2.2 bus
- Optional custom bus

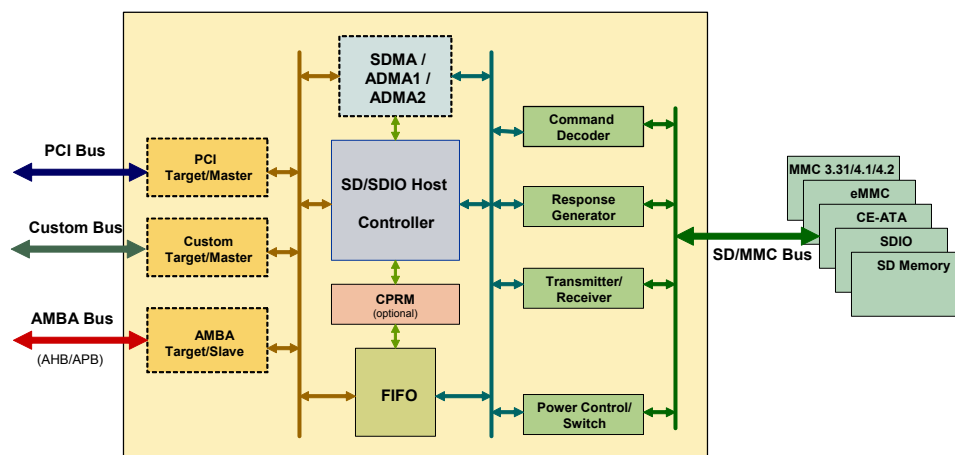
Overview

The Arasan SD/MMC/CE-ATA Host IP Core (CE-ATA 2) is the world's first integrated IP core with support for the SD 2.0, SDIO 2.0, MMC4.2, eMMC (MMC4.3), and CE-ATA 1.1 controllers. The IP supports host interfaces including AHB, APB, PCI, and other custom buses. It is designed to support SD / SDIO / MMC / CE-ATA multimedia applications in handheld and consumer electronic devices.

The Arasan CE-ATA 2 Host IP Core is fully compliant with the SD Host specification version 2.0 with Advanced-DMA support, MMC specification version 4.2, eMMC, and CE-ATA Digital Protocol revision 1.1RC. The IP supports SPI, SD 1-bit, SD 4-bit, MMC 8-bit modes. The CE-ATA 2 Host IP Core is designed to support high-speed and full-speed SD data transfers. In applications with an AHB interface, the CE-ATA 2 Host IP core communicates with the ARM processor at a clock speed of up to 300 MHz. The CE-ATA 2 Host controller includes a DMA controller and a FIFO that is expandable from a minimum size of 4 x 32-bit. An optional CPRM functional block can be incorporated to perform a cipher algorithm for encryption and decryption.

The CE-ATA 2 Host IP Core is an RTL design in Verilog that implements an SD/MMC/CE-ATA host controller on an ASIC, or FPGA. The core includes RTL code, test scripts and a test environment for verification. The Arasan CE-ATA 2 Host IP Core has been widely used in different SDIO applications by major chip vendors with proven silicon. Also available are the Arasan SD Host Hardware Development Kit (HDK) and SD Host Hardware Validation Platform (HVP).

SD/MMC/CE-ATA Host IP Core Functional Block Diagram



SD/MMC/CE-ATA Host IP

SD/SDIO Interface:

The SD 2.0, SDIO 2.0, MMC3.31/4.1/4.2, eMMC, and CE-ATA devices communicate with the host controller through the SD/MMC Bus Interface Unit (BIU). The BIU consists of the Command Decoder, Response Generator, Transmitter/Receiver, and Power Control/Switch units. SD1, SD4 and SPI modes are supported. Other BIU functions includes the 16-bit CRC generator and checker for the data lines, 7-bit CRC generator and checker for the command and response lines, interrupt state machine, and BIU master state machine.

MMC/CE-ATA Interface:

The MMC interface conforms with the MMC system specification 3.31, 4.1, 4.2, and 4.3. It supports 8-bit MMC mode, power-on boot mode, sleep mode, Error Correction Code (ECC), MMCplus, and MMCmobile card types. The CE-ATA Host Controller IP conforms with CE-ATA Digital Protocol revision 1.1RC, with support for CE-ATA Digital Protocol commands (CMD39 / CMD60 / CMD61). The CE-ATA interface allows for lower pin count, better power utilization, voltages tailored to battery-based applications, and more efficient command protocol.

Advanced DMA:

The controller supports SDMA, ADMA1 and ADMA2. The Single Operation DMA (SDMA) algorithm interrupts at every page boundary. ADMA adopts a scatter-gather DMA algorithm to increase data transfer speeds. ADMA provides data transfer between

system memory and SD card without interruption of a CPU execution. ADMA supports 32-bit system memory addressing. ADMA1 supports data transfer of 4KB aligned data in system memory. ADMA2 being more flexible in supporting data of any location and any size to be transferred in system memory.

AHB/APB Interface:

The Arasan SD/MMC/CE-ATA Host IP Core provides a Programmed I/O method in which the ARM host driver transfers data using the Buffer Data Port register. The AHB slave has direct access to the Host Control registers and these registers can be programmed by the ARM processor through the AHB slave interface. Data transactions are performed through the AHB slave interface with Programmed I/O method. The AHB Interface initiates a read or write transaction with the memory if the data transaction is an DMA data transfer.

Optional and Custom Interfaces:

PCI Target/Master can be implemented that conforms to PCI specifications 2.2. General purpose buses such as 8-bit and 16-bit parallel buses are optional modules. Custom buses with special requirements can also be implemented.

Host Hardware Validation Platform (HVP):

The HVP is designed for validation and compliance testing of SD host devices .



Host Hardware Development Kit (HDK):

The HDK is a PCI plug-in card for SD host prototyping and driver development.



Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Items:

- Host Hardware Development Kit (HDK)
- Host Hardware Validation Platform (HVP)
- SD/MMC/CE-ATA Linux stack

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

SD/MMC/CE-ATA Host IP Core:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com

