

SD 2.0 Memory Controller

Features

- Meets SD 2.0 Physical Layer Specification
- Supports SPI, 1-bit, and 4-bit SD modes
- Supports SDHC and SDHS cards
- 0-50 MHz host clock rate
- CRC7 for command and CRC16 for data integrity
- Card locking, write protection and password features supported
- NAND Flashes used as storage memory area
- Memory size from 128MB to 2GB
- Supports 512/1024/2048 bytes block lengths or sector sizes
- Programming through CPU interface
- Flexible architecture to handle sophisticated wear leveling, garbage collection and bad block management for NAND flashes in firmware
- ECC using hamming code algorithms handled in the firmware
- Built-in FIFOs for data-out and data-in paths
- Works with the default FATFS driver for SD memory in all platforms

Overview

The SD memory card (Secure Digital memory card) provides high-speed low-power data storage and access for mobile electronic devices. SD card is designed to meet the security, capacity, performance and environmental requirements that inherent in newly emerging audio and video consumer electronic devices.

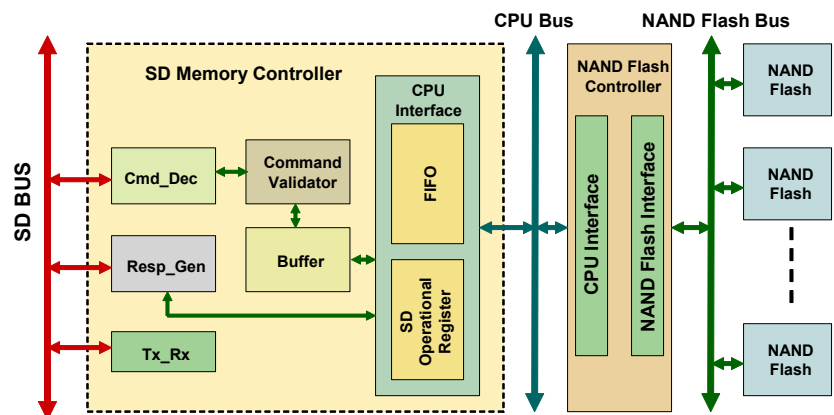
The Arasan SD 2.0 Memory Controller IP Core can be used with any type of flash memory interfaces. The core supports card locking, write protection and password features. The SD 2.0 Memory Controller card supports hot insertion or removal. It operates at 0-52 Mhz input clock

The IP core includes a Command Decoder (cmd_dec) that interprets the 48-bit commands. The Response Generator (Resp_gen) generates appropriate responses to answer the incoming commands. Abort protocol is supported. The Command Validator (Cmd_valdr) validates the received command based on the state of the card and checks for errors. It also handles password authentications and the checking of locked/unlocked state of the card. The SD Operational register set holds the OCR, CID, CSD, DSR, SCR, and RCA for the SD card. The Sector Buffer inside the FIFO has a size of 2048 x 8 bytes that supports up to a 2k page size.

An optional NAND flash memory controller can be used for connecting the SD controller to the flash devices. A DMA controller can be included to transfer data between the SD and flash interfaces. The NAND Flash Controller consists of the CPU interface, NAND flash interface, and Operational registers.



SD 2.0 Memory Controller Functional Block Diagram



The Arasan SD 2.0 Memory Controller IP Core is an RTL design in Verilog that implements an SD 2.0 Memory Controller controller on an ASIC or FPGA. The core includes RTL code, test scripts and a test environment for full simulation verifications.

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SD Bus Interface:

The SD Bus interface supports SD1, SD4, and SPI transfer modes. The SD Bus interface consists of the Command Decoder (Cmd_Dec), Response Generator (Resp_Gen), and Transmitter/Receiver (Tx_Rx). The Command Decoder (cmd_dec) interprets the 48-bit commands in all modes (SPI, SD 1-bit and SD 4-bit). This block checks for CRC of the commands. The Response Generator (Resp_gen) generates appropriate responses to answer the incoming commands. The Transmitter/Receiver (Tx_rx) block handles data transactions for all modes. This block controls the data lines of the SD bus. Abort protocol is supported.

SD Controller Logic:

The Command Validator (Cmd_valdr) validates the received command based on the state of the card. This block checks for parameter errors, address errors and all errors in the argument field of the command. It also handles password authentications and checks for locked/unlocked state of the card.

The Bus_state_machine handles the SD bus states as mentioned in the physical layer specification 2.0.

CPU Interface:

The CPU interface consists of an internal FIFO and the SD Operational Registers. An internal FIFO holds the temporary receive and transmit data. The receive FIFO holds

received bytes before sending it to the flash memory. The transmit FIFO holds the bytes to be transmitted. A Sector Buffer, which is part of the FIFO, has a size of 2048 x 8 bytes. The Sector Buffer can be used to support up to a 2k page size. The SD Operational registers holds the OCR, CID, CSD, DSR, SCR, and RCA for the SD memory card.

NAND Flash Controller:

In applications when a NAND Flash controller is needed, The Arasan NAND Flash Controller IP can be used. The controller consists of the CPU interface, Operational registers, and NAND Flash Interface. The Operational registers holds the registers essential to program the Flash controller. Controlling functions include identifying the type of flash that it needs to support, supporting commands for operation of the flash, and setting of page buffer size.

Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Technical documents

Optional Items:

- SD Memory Development Board
- Linux stack

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog



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Data Sheet Links:

SD 2.0 Memory IP Core:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com