

Features

- Complies with Physical Layer Specification Version 3.0
- SDXC cards have a capacity from 32GB up to 2TB
- Supports SDR12, SDR25, SDR50, SDR104 and DDR50
- Implements UHS-I cards with a peak bandwidth in SDR up to 104MB/s, DDR up to 50MB/s
- Supports SPI, 1-bit and 4-bit SD data bus
- Sector address allows host to access high capacity card
- Correction of memory field errors
- Comfortable erase mechanism.
- Multiple Card data protection modes - power on, temporary, permanent and password based
- Supports Switch Function to expand card functionality
- Hardware based CRC checking
- CRC7 for Command and CRC16 for Data integrity
- Supports block lengths or sector sizes of 512, 1024 and 2048 bytes
- Clock control for low power

AHB

- Complies to AMBA specification version 2.0.
- Supports incremental burst transfers in DMA mode
- Supports register transfer in non-DMA mode
- Supports retry and split

SDXC Memory Controller IP

Overview

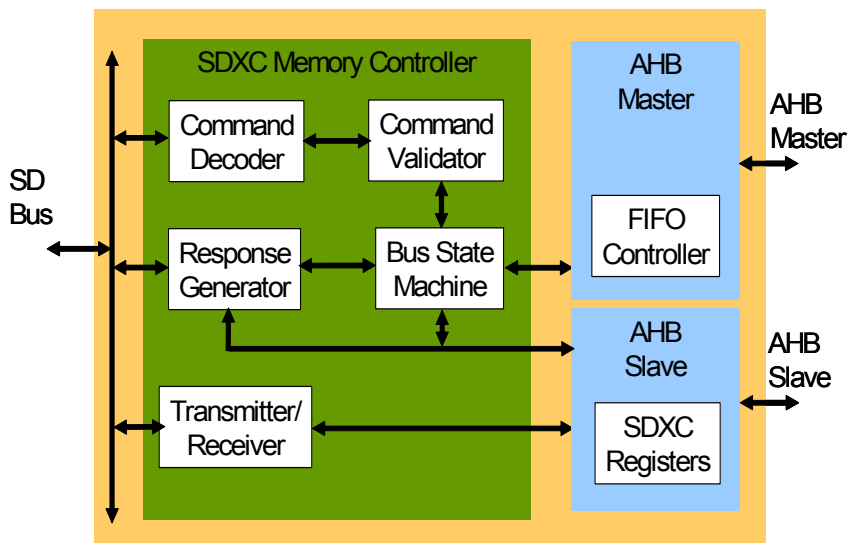
Secure Digital eXtended Capacity (SDXC) is the latest specification released by the SD Association. SDXC memory cards can store between 32GB to 2TB of data and have a peak memory bandwidth of 104MBps. These cards are geared to meet the performance, capacity, security and power requirements of the next generation of consumer electronics products. Arasan’s SDXC Memory Controller IP is easily adapted to interface with new NAND Flash technologies that can scale to meet the capacity and performance of SDXC.

Arasan’s SDXC Memory Controller IP is compliant with the Physical Layer Specification Version 3.0 (SDXC). The controller supports Ultra-High Speed (UHS-I) mode with a peak bandwidth of 104Mbps. It can be used with multiple types of NAND Flash technology. The core supports all of the standard SD security features such as write protection schemes, password protected card locking as well as authentication based content protection. The controller detects the insertion or removal of the card and ensures data is not altered when removed during read access.

The SDXC Memory Controller is designed to operate at a maximum frequency of 208 MHz. The interface supports SPI, SD 1-bit and 4-bit modes. The controller provides hardware support for all of the data protection schemes in the SDXC standard including password verification and management. The controller handles block lengths or sector sizes of 512, 1024 and 2048 bytes. Cyclic redundancy code calculation is performed in hardware and is used to detect errors in the data stored in the memory. CRC 7 is used as the CRC for commands and CRC 16 bit is used for data.

Arasan provides a “Total IP Solution” for the SDXC Memory Controller consisting of RTL source files, synthesis scripts, test environment which are backed by our World-class customer support.

SDXC Memory Controller IP Core Functional Block Diagram



SDXC Memory Controller IP

SDXC Memory Controller:

This block comprises of the Command Decoder, Command Validator, Response Generator, Receiver, Transmitter, and Bus State Machine. The Command Decoder registers the 48-bit command for all modes including SPI, SD 1-bit and 4-bit modes. It also verifies the CRC for received commands. The Response Generator sends appropriate responses for commands received in all modes. The Transmitter and Receiver handle data transactions in all modes. Abort protocol is supported. The Command Validator validates received commands based on the state of the controller. This block checks for parameter errors, address errors and errors in the argument field of the command. It also handles password authentications and verifies whether the card is locked or unlocked. The Bus State Machine handles bus states described in the SDXC Physical Layer Specification.

Related Products

Arasan has an extensive portfolio of SDXC compatible Host Controllers. Software stacks are also available for these IP cores.

AHB/APB Interface:

The AHB interface consists of the master interface and slave interface. The AHB slave is used by external processor to configure the SDXC Memory Controller, and for programming the control of data transfer between the controller and application memory. The AHB master interface is used to transfer packets between the internal FIFOs and application memory. Before an AMBA AHB transfer can commence, the bus master must be granted access to the bus. This process is started by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted the use of the bus. A granted bus master starts an AHB transfer by driving the address and control signals.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Reuse Methodology Manual guidelines (RMM) compliant verilog code

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Related Products

- Arasan has a complete portfolio of SDXC Host Controllers and associated Software Stacks



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