

Features

SD 3.0 (SDXC)

- Complies with Physical Layer Specification Version 3.0
- Supports SPI, 1-bit, 4-bit SD modes
- Implements UHS-I with a peak bandwidth of 104MBps
- Supports SDR12, SDR25, SDR50, SDR104 and DDR50
- Addresses memory capacity of up to 2TB
- Card locking, write protection and password based data protection are supported

MMC 4.4 (eMMC)

- Complies to Multimedia Card System Specification Version 4.4 (eMMC)
- 1-, 4-, or 8-bit MMC data bus
- DDR mode peak bandwidth upto 104MBps
- Controller supports hardware reset pin (RST_n)
- Flexible Partition Management features with enhanced storage option
- Accesses over 2GB memory
- Supports both Power-on boot mode and alternate boot mode
- Sector address allows host to access high capacity card
- Performs Secure Erase, Secure TRIM and TRIM operations
- Replay Protected Memory Block (RPMB) to enhances security

Common Features

- Card write protection (power on, temporary and permanent) and password features
- Supports block lengths or sector sizes of 512, 1024, and 2048 bytes
- Hot insertion of cards
- Memory error correction mechanisms

AHB

- Complies to AMBA specification version 2.0.
- Supports incremental burst transfers in DMA mode
- Supports register transfer in non-DMA mode
- Supports retry and split

SD 3.0 / eMMC 4.4 Memory Controller IP

Overview

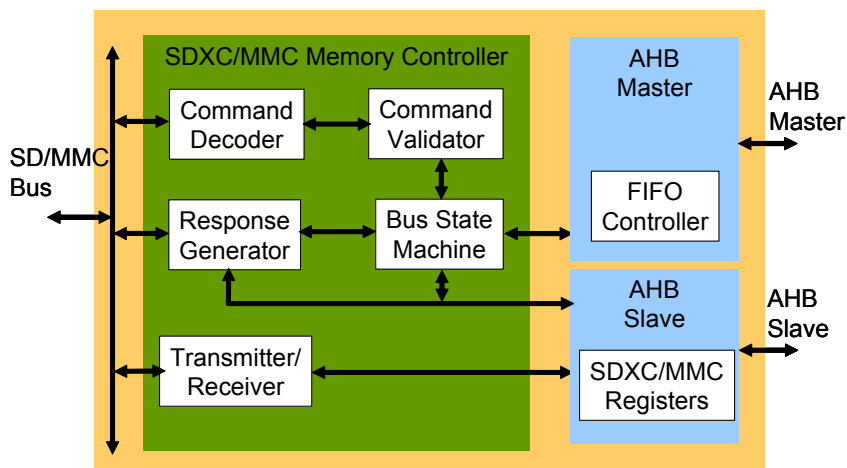
The rapid growth in features and functionality of compact and portable electronics has resulted in the increasing use of the Secure Digital (SD) or MultiMedia Card (MMC) interface for embedded or removable data storage. Arasan's SD / eMMC Memory Controller IP Core can be used by memory card designers to interface with either standard.

Arasan's SD / eMMC Memory Controller IP is compliant with the SD Physical Layer Specification 3.0 and the MMC 4.4 (eMMC) standard. The controller supports a peak bandwidth of 104MBps. A NAND Flash storage device can be connected to the AHB bus on this Memory Controller using a NAND Flash controller (also available from Arasan). The SD / eMMC Memory controller simplifies accessing NAND Flash memory by abstracting the differences amongst various NAND Flash architectures. The controller supports all of the SD features such as content protection, write protection, correction of memory errors and password based card locking and un-locking.

The SD / eMMC Memory Controller operates at a maximum frequency of 208 MHz. The interface supports SD 1-bit, 4-bit modes and MMC 1-bit, 4-bit, and 8-bit modes. The Memory Controller supports the newer eMMC functions such as multiple boot mechanisms, flexible card memory partitions, replay protected memory block and secure erase. eMMC can be used for power-on booting without the need for a software driver. The explicit sleep mode allows the host to instruct the controller to directly enter the sleep mode. The controller supports block lengths or sector sizes of 512, 1024 and 2048 bytes.

Arasan provides a "Total IP Solution" for the SD / eMMC Memory controller by providing RTL source files, synthesis scripts, test environment and documentation which are backed by Arasan's World-class support.

SD 3.0 / eMMC 4.4 Controller IP Core Functional Block Diagram



SD 3.0 / eMMC 4.4 Memory Controller IP

SD / eMMC Controller:

The controller comprises of the Command Decoder, Command Validator, Response Generator, Receiver, Transmitter, and Bus State Machine. The Command Decoder registers the 48-bit command for all modes including MMC 1-bit, 4-bit, and 8-bit modes. It also verifies the CRC for received commands. The Response Generator sends appropriate responses for received commands in all modes of operation. The Transmitter and Receiver block handles the data transactions. Abort protocol is supported. The Command Validator validates the received commands based on the state of the controller. This block checks for parameter errors, address errors and errors in the argument field of the command. It also handles password authentications and is responsible to check if the card is locked or unlocked. The Bus State Machine handles bus states described in the SD, eMMC card specification. The eMMC compliant controller sup-

ports additional features such as power-on boot mode, sleep mode, and sector address mapping for high-capacity card access.

AHB/APB Interface:

The AHB interface consists of the master interface and slave interface. The AHB slave is used by external processor to configure the SD / eMMC Memory controller, and for programming the control of data transfer between the it and application's memory. The AHB master interface is used to transfer packets between the internal FIFOs and application memory. Before an AMBA AHB transfer can commence, the bus master must grant access to the bus. This process is started by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted the use of the bus. A granted bus master starts an AHB transfer by driving the address and control signals.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Reuse Methodology Manual guidelines (RMM) compliant verilog code

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents



Arasan Chip Systems, Inc.

2010 N. First St. Suite #510
San Jose CA 95131
Phone: 408-282-1600
Fax: 408-282-7800
E-mail: sales@arasan.com

Data Sheet Links:

<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com