

ATA Controller IP Core

Overview

The Advanced Technology Attachment (ATA) is a proven standard to interconnect hard disk drives (HDD), solid state drives (SSD), CD/DVD-ROM and other media to a host system. The parallel interface of the ATA is also referred to as PATA and enables multiple disk drives to be connected over a flexible cable in a cost effective manner.

Arasan's ATA IP core supports the ATA/ATAPI-6 standard. This standard extends the Logical Block Addressing to 48 bits enabling the host to interface with larger capacity drives. The controller directly interfaces to an ATA/ATAPI on the device side and supports a native AHB target bus interface on the application side for easy integration into an SoC.

The AHB interface is used by the host to program the Control Registers and generate transactions on the ATA interface. A FIFO inside the Transaction Controller is used as a temporary storage to provide efficient support for various DMA modes. The ATA controller supports a background access function which greatly reduces the host processors load for transferring bulk data.

Arasan's ATA IP is available in RTL format and can be implemented either on an FPGA or an ASIC. The design collateral provided with this IP includes the RTL code, documentation and a complete test and verification environment.

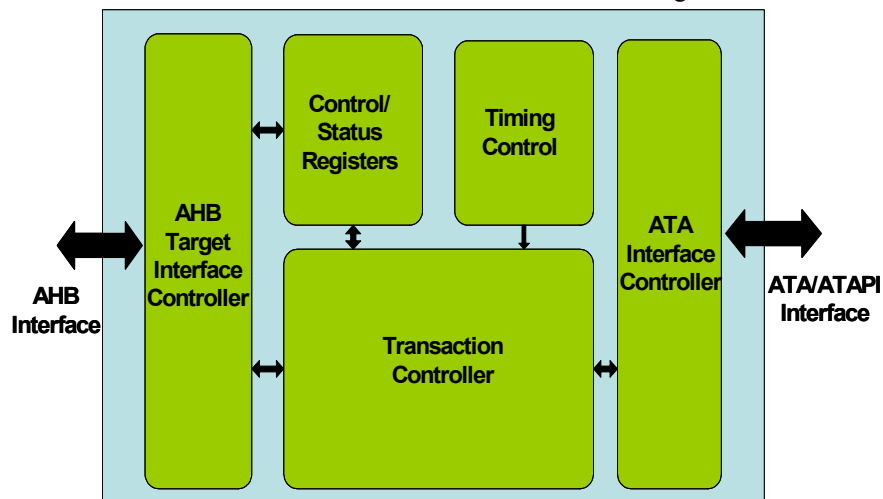
Features

- Compliant with ATA/ATAPI-6
- Supports up to two devices in Master / Slave configuration on the ATA bus
- Independent timing modes for each device
- Dual clock architecture to permit ATA Interface to execute independent of AHB
- Direct access to ATA register set eases initialization of drives
- Flexible data transfer modes
- PIO Mode
 - Mode0 through Mode6
- Multi-word DMA Mode
 - Mode0 through Mode4
- Ultra DMA Mode
 - Mode0 through Mode6

Host Interface

- AHB Bus for data transfer
- AHB slave Bus for register access

ATA Controller IP Core - Functional Block Diagram



ATA Controller IP Core

Functional Blocks:

ATA Interface Controller:

This block interfaces with the ATA interface signals and performs PIO or DMA transfers based on the instructions from Transaction Controller. The Interface Controller block deals with single PIO or DMA Burst transfer at a time, while the Transaction Controller maintains the overall Transfer Counts. The Interface Controller also gets the timing information from the Timing Controller block and uses this timing information when performing PIO or DMA transfers.

Transaction Controller:

The Transaction Controller implements the main control logic for the ATA controller and manages the generation of transaction sequence on the ATA Interface. Based on the current transfer mode for e.g., PIO, Multi-Word DMA or UltraDMA, the controller generates the appropriate transfer sequence to the ATA Interface Controller when the Transfer Control Register is programmed to initiate transfer.

Timing Control:

The Timing Control block is used to generate the timing information for the ATA Interface. The timing information is based on the frequency of the interface clock and the current timing mode of the ATA Device. The timing information is critical for the correct operation of the ATA controller when generating transfers on the ATA Interface. The timing information is hard coded in this block based on the timing values documented in the ATA specification.

Control / Status Register:

The Control and Status Registers Block contains a set of registers that are used for the operation of the ATA controller. These registers include the configuration and status registers, etc. This block also provides access to ATA register set in the ATA device when operating in PIO Mode. In addition, this block generates an interrupt to the cpu that is triggered by various monitoring events.

Host Interface:

The AHB interface is a target interface used by the host to configure and initiate ATA/ATAPI transactions. The configuration includes the setting up of various DMA modes.

Benefits:

- Fully compliant core
- Premier direct support from Arasan IP core designers
- Easy to use industry standard test environment
- Un-encrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy to use test environment
- Synthesis scripts
- Technical documents

Supported Tools:

- Simulation: ModelSim, NC-Verilog, VCS
- Synthesis: Synopsys Design Compiler



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Data Sheet Links:

ATA Controller IP Core:
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:
www.arasan.com