

## SD / SDIO / eMMC Host Controller IP

### Features

- **Memory Card / Form Factors**
  - SD Host Controller Spec v3.0 (SDXC)
  - SDIO Spec v3.0
  - SD Memory Spec v3.0
  - eSD Memory Spec v2.1
  - eMMC Spec v4.4
  
- **IP Details**
  - Built-in Master DMA for efficient data transfer
  - Supports single slot. Optional support for multiple slots
  - Power-on boot mode
  - Optional bus support - AXI, OCP, BVCI, custom
  - Detect card insertion and removal during power down or clock turn-off
  - Optional SPI mode support to handle legacy SD, MMC cards
  - SD - Secure Digital Memory Card
    - SDSC, SDHC, SDXC cards
    - 25/50/104/208 MHz
    - 1,4 bit of data
  - SDIO - SD Input/Output
    - 25/50/104/208 MHz
    - 1,4 bit of data
  - eMMC - MultiMedia Card
    - 26/52/52 MHz
    - 1,4,8 bit of data
  
- **End Products**
  - SSD - Solid State Drives
  - Picture frames
  - Laptops
  - Printers
  - Digital Cameras
  - Smart Phones
  - Games Consoles

### Overview

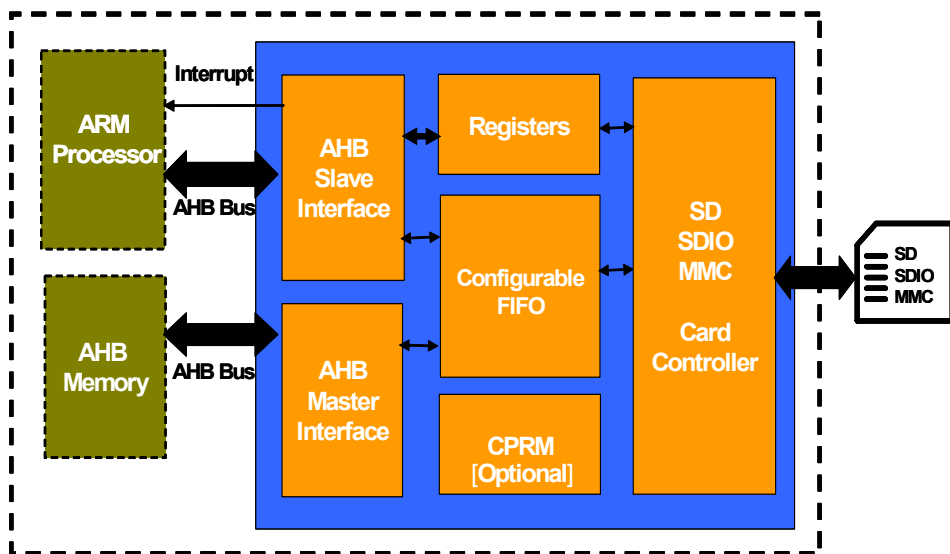
As the mobile industry continues to grow, the requirements for both internal and external memory are increasing at an exponential rate. At the system level, memory interfaces with larger capacities, smaller form factor and faster access times in addition to support for multiple industry standards are needed.

Arasan Chip Systems' SD / SDIO / eMMC IP is a highly integrated host controller IP solution that supports three key memory and I/O technologies: 1) SDXC, 2) SDIO and 3) eMMC memory formats. This IP handles all of the timing and interface protocol requirements to access these media as well as processing the commands in hardware thereby scaling in both performance and access speeds.

The IP supports connection to a single slot and performs multi-block writes and erases that lower access overhead. In addition, a host can utilize this IP to boot directly from an attached eMMC memory, thereby simplifying system initialization during power up. The host interface is based on a standard 32-bit AHB bus which is used to transfer data and configure the IP.

Arasan's thorough verification methodology takes the risk out of integration of this functionality. As an Executive Member of the SD Association and a member of JEDEC, Arasan is a leading provider of quality IP ensuring SoC designers risk-free integration of this advanced functionality. In addition to this SD / SDIO / eMMC IP core, Arasan provides a family of different memory solutions to address a variety of needs. Arasan provides verification IP, test environment and a hardware development kit to ease integration into an SoC.

SD / SDIO / eMMC IP Block Diagram



# SD / SDIO / eMMC Host Controller IP

## SD / SDIO / eMMC Controller

The SD / SDIO / eMMC IP core is an integration of key industry memory and storage specifications into a single solution. Optimized for size and performance, it shares common functional blocks to minimize the size implementation. It can support embedded or (optionally) multiple external slots. A variety of host interfaces can also be supported. This IP supports SD/SDIO and the eMMC card formats.

## SD, eMMC Memory Card Controller

Arasan's SD (Secure Digital) and eMMC (MultiMedia Card) controllers provides high-speed, low-power data storage and access. The controller interfaces with SDSC, SDHC, SDXC as well as eMMC cards. It supports card locking, write protection, password features, and hot insertion or removal. The SD interface operates up to 204MHz and supports all SD bus modes - SPI, SD 1-bit, and SD 4-bit modes. The eMMC interface operates up to 52MHz and supports - SPI, eMMC 1-bit, eMMC 4-bit and eMMC 8-bit bus widths.

## SDIO Card Controller

With complete support for SDIO cards, this

Host controller can be used to connect cards with IO functionality, thereby extending the capability of the platform to support applications such as Wimax, Wireless USB, GPS that are not part of the base platform.

## Advanced DMA

The controller supports SDMA, ADMA1 and ADMA2. The Single operation DMA (SDMA) interrupts the host cpu at every page boundary while the ADMA uses a scatter gather DMA algorithm to reduce the load on the host cpu. It supports both 32-bit and 64-bit system memory addressing. ADMA2 improves upon ADMA1 by removing restrictions on data location and size.

## Target Applications

Primarily focused on mobile applications requiring memory controllers such as smart-phones portable multimedia devices, netbooks, Arasan's SD / SDIO / eMMC IP is also applicable to product categories such as picture frames, cameras, printers, MIDs, UMDs, PDAs and other consumer electronics.

## Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- Reuse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spy-glass

## Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

## Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux, WinCE, and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

## Related Products:

- SD / SDIO / eMMC Host Software Stack
- SD / SDIO / eMMC HDK (in development)
- Other Host Controller IP



## Various Multi-card Applications



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## Data Sheet Links:

Memory & Storage IP Core data sheets:  
<http://www.arasan.com/datasheets/login.php>

For a complete directory of Arasan IPs, please visit:  
[www.arasan.com](http://www.arasan.com)

